

Jianhua (Joshua) Yang

Department of Electrical and Computer Engineering
University of Massachusetts, Amherst
201G Marcus Hall, 100 Natural Resources Rd
Amherst MA 01003-9292

e-mail: jjyang@umass.edu

Tel: 413-5454514

<http://www.ecs.umass.edu/ece/jjyang/>

Employment Experience:

Professor, 2015-

The Department of Electrical and Computer Engineering
University of Massachusetts, Amherst

Principal Researcher, 2012-2015

Responsibility: Leading the materials team
Senior Researcher, Researcher, Research Associate (post-doctoral), 2007-2012
Hewlett-Packard Labs, Palo Alto, CA

R&D Engineer, 2000-2001

Huawei Technologies Co., Ltd., a world-leading telecommunication solution provider

Education:

Ph. D., M.S., Materials Science Program, 2007

University of Wisconsin – Madison

Advisor: Y. Austin Chang (Deceased, member of National Academy of Engineering)

Thesis: Engineering and Characterizing Nanoscale Multilayers for Magnetic Tunnel Junctions (MTJs)

B.S. Mechanical Engineering, 1997

Southeast University, Nanjing, China

Selected publications: (*corresponding author; full list in [Google Scholar](#))

1. Z. Wang, M. Rao, J.-W. Han, J. Zhang, P. Lin, Y. Li, C. Li, W. Song, S. Asapu, R. Midya, Y. Zhuo, H. Jiang, J. H. Yoon, N. K. Upadhyay, S. Joshi, M. Hu, J. P. Strachan, M. Barnell, Q. Wu, H. Wu, Q. Qiu, R. S. Williams, Q. Xia^{*}, and **J. Joshua Yang^{*}**, “Capacitive neural network with neuro-transistors”, *NATURE COMMUNICATIONS* **9** 3208 (2018).
2. C. Li, D. Belkin, Y. Li, P. Yan, M. Hu, N. Ge, H. Jiang, E. Montgomery, P. Lin, Z. Wang, J. P. Strachan, M. Barnell, Q. Wu, R. S. Williams, **J. Joshua Yang^{*}**, and Q. Xia^{*}, “Efficient and self-adaptive in-situ learning in multilayer memristive neural networks”, *NATURE COMMUNICATIONS* **9**, 2385 (2018).
3. Z. Wang, S. Joshi, S. Savel’ev, W. Song, R. Midya, Y. Li, M. Rao, P. Yan, S. Asapu, Y. Zhuo, H. Jiang, P. Lin, C. Li, J. H. Yoon, N. K. Upadhyay, J. Zhang, M. Hu, J. P. Strachan, M. Barnell, Q. Wu, H. Wu, R. Stanley Williams^{*}, Q. Xia^{*}, and **J. Joshua Yang^{*}**, “Fully memristive neural networks for inference and unsupervised learning”, *NATURE ELECTRONICS* **1**, 137-145 (2018).
4. Z. Wang, S. Joshi, S. E. Savel’ev, H. Jiang, R. Midya, P. Lin, M. Hu, N. Ge, J. P. Strachan, Z. Li, Q. Wu, M. Barnell, G-L Li, H. L. Xin, R. S. Williams, Q. Xia, and **J. Joshua Yang^{*}**,

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- “Memristors with diffusive dynamics as synaptic emulators for neuromorphic computing”, *NATURE MATERIALS* **16**, 101-108 (2017).
5. C. Li, M. Hu, Y. Li, H. Jiang, N. Ge, E. Montgomery, Z. Li, J. P. Strachan*, P. Lin, W. Song, Z. Wang, M. Barnell, Q. Wu, R. S. Williams, **J. Joshua Yang***, Q. Xia*, “Analogue signal and image processing with large memristor crossbars”, *NATURE ELECTRONICS* **1**, 52-59 (2017).
 6. M. Hu, C. E. Graves, C. Li, Y. Li, N. Ge, E. Montgomery, N. Davila, H. Jiang, R. S. Williams, **J. Joshua Yang***, Qiangfei Xia*, and John Paul Strachan*, “Memristor-based analog computation and neural network classification with a dot product engine”, *ADVANCED MATERIALS* **29**, 1705914 (2018).
 7. J. H. Yoon, Z. Wang, K. M. Kim, H. Wu, V. Ravichandran, Q. Xia*, C. S. Hwang and **J. Joshua Yang***, “An Artificial Nociceptor Based on a Diffusive Memristor”, *NATURE COMMUNICATIONS* **9**, 417 (2018).
 8. M. Wang, S. Cai, C. Pan, C. Wang, X. Lian, K. Xu, Y. Zhuo, **J. Joshua Yang***, P. Wang*, F. Miao*, “Robust memristors based on layered two-dimensional materials”, *NATURE ELECTRONICS* **1**, 130-136 (2018).
 9. Z. Wang, M. Rao, R. Midya, S. Joshi, H. Jiang, P. Lin, W. Song, S. Asapu, Y. Zhuo, C. Li, H. Wu*, Q. Xia*, and **J. Joshua Yang***, “Threshold Switching of Ag or Cu in dielectrics: Materials, Mechanism, and Applications”, *ADVANCED FUNCTIONAL MATERIALS* **28**, 1704862 (invited feature article, 2018).
 10. **J. Joshua Yang*** and Q. Xia*, “Battery-like artificial synapses”, *NATURE MATERIALS* **16**, 396-397 (2017).
 11. R. Midya, Z. Wang, J. Zhang, C. Li, S. Joshi, H. Jiang, P. Lin, K. Norris, N. Ge, Q. Wu, M. Barnell, Z. Li, R. S. Williams, Q. Xia*, and **J. Joshua Yang***, “Anatomy of Ag/hafnia based selectors with 10^{10} nonlinearity”, *ADVANCED MATERIALS* **29**, 1604457 (2017).
 12. J. H. Yoon, J. Zhang, X. Ren, Z. Wang, H. Wu, Z. Li, M. Barnell, Q. Wu, L. J. Lauhon, Q. Xia and **J. Joshua Yang***, “Truly Electroforming-Free and low- Energy Memristors with Pre-conditioned Conductive Tunneling Paths”, *ADVANCED FUNCTIONAL MATERIALS* **27**, 1702010 (2017).
 13. H. Jiang, D. Belkin, S. Savel'ev, S. Lin, Z. Wang, Y. Li, S. Joshi, R. Midya, C. Li, M. Rao, M. Barnell, Q. Wu, **J. Joshua Yang***, Q. Xia*, “A novel true random number generator based on a stochastic diffusive memristor”, *NATURE COMMUNICATIONS* **8**, 882 (2017).
 14. C. Li, L. Han, H. Jiang, M. Jang, **J. Joshua Yang**, H. L. Xin and Q. Xia*, “3-Dimensional Crossbar Arrays of Self-rectifying Si/SiO₂/Si Memristors”, *NATURE COMMUNICATIONS* **8**, 15666 (2017).
 15. Ch. Wu, T. W. Kim, H. Y. Choi, D. U. Lee, D. R. Strukov and **J. Joshua Yang**, “flexible 3D artificial synapse networks with correlated learning and trainable memory capability”, *NATURE COMMUNICATIONS* **8**, 752 (2017).
 16. Ch. Wu, T. W. Kim, T. Guo, F. Li, D. U. Lee, and **J. Joshua Yang**, “Mimicking classical conditioning based on a single flexible memristor”, *ADVANCED MATERIALS* **29**, 1602890 (2017).
 17. B. J. Choi, J. Zhang, K. Norris, G. Gibson, K. M. Kim, W. Jackson, M. Zhang, Z. Li, **J. Joshua Yang***, and R. Stanley Williams*, “Trilayer Tunnel Selectors for Memristor Memory Cells”, *ADVANCED MATERIALS* **28**, 356-362 (2016).
 18. B. J. Choi, A. C. Torrezan, J. P. Strachan, P. G. Kotula, A. J. Lohn, M. J. Marinella, R. S. Williams* and **J. Joshua Yang***, “High-speed and low-energy nitride memristors”, *ADVANCED FUNCTIONAL MATERIALS* **26**, 5290-6296 (2016).

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19. B. J. Choi, A. C. Torrezan, K. J. Norris, F. Miao, J. P. Strachan, M.-X. Zhang, D. A. A. Ohlberg, N. P. Kobayashi, **J. Joshua Yang***, and R. S. Williams, “Electrical performance and scalability of Pt dispersed SiO₂ nanometallic resistance switch”, *NANO LETTERS* **13**, 3217 (2013).
 20. **J. Joshua Yang***, Dmitri B. Strukov and Duncan R. Stewart, “Memristive devices for computing”, *NATURE NANOTECHNOLOGY* **8**, 13 (2013).
 21. **J. Joshua Yang***, M.-X. Zhang, M. D. Pickett, F. Miao, J. P. Strachan, W. Li, W. Yi, D. A. A. Ohlberg, B. J. Choi, W. Wu, J. H. Nickel, G. Medeiros-Ribeiro and R. Stanley Williams, “Engineering nonlinearity into memristors for passive crossbar applications”, *APPLIED PHYSICS LETTERS* **100**, 113501 (2012).
 22. F. Miao, J. P. Strachan, **J. Joshua Yang***, M.-X. Zhang, I. Goldfarb, A. C. Torrezan, P. Eschbach, R. D. Kelley, G. Medeiros-Ribeiro and R. S. Williams “Anatomy of a nanoscale conduction channel reveals the mechanism of a high-performance memristor”, *ADVANCED MATERIALS* **23**, 5633 (2011).
 23. J. Borghetti, G. S. Snider, P. J. Kuekes, **J. Joshua Yang**, D. R. Stewart and R. S. Williams “‘Memristive’ switches enable ‘stateful’ logic operations via material implication”, *NATURE* **464**, 873 (2010).
 24. **J. Joshua Yang**, J. P. Strachan, Q. Xia, D. A. A. Ohlberg, P. J. Kuekes, R. D. Kelley, W. F. Stickle, D. R. Stewart, G. Medeiros-Ribeiro, R. S. Williams, “Diffusion of adhesion layer metals controls nanoscale memristive switching”, *ADVANCED MATERIALS* **22**, 4034 (2010).
 25. **J. Joshua Yang***, M.-X. Zhang, John Paul Strachan, Feng Miao, Matthew D. Pickett, Ronald D. Kelley, G. Medeiros-Ribeiro, R. Stanley Williams “High switching endurance in TaO_x memristive devices”, *APPLIED PHYSICS LETTERS* **97**, 232102 (2010).
 26. **J. Joshua Yang**, J. Borghetti, D. Murphy, D. R. Stewart and R. S. Williams “A family of electronically reconfigurable nanodevices”, *ADVANCED MATERIALS* **21**, 3754 (2009).
 27. **J. Joshua. Yang**, F. Miao, D. Ohlberg, D. Stewart, R. S Williams “Electroforming mechanism of metal/oxide/metal memristive switches”, *NANOTECHNOLOGY* **20**, 215201(2009).
 28. **J. Joshua Yang**, M. D. Pickett, X. Li, D. A. A. Ohlberg, D. R. Stewart, and R. S. Williams “Memresistive switching mechanism for metal/oxide/metal nano-devices” *NATURE NANOTECHNOLOGY* **3**, 429 (2008).

Patents:

94 Granted patents (see detailed publication list) and **over 70** pending patents (documents available upon request) with USPTO. Two patents on MRAM were licensed by Intel for **millions of dollars** through UW-Madison and the patents on ReRAM/Memristor were **transferred** to SK-hynix (2nd largest memory manufacturer in the world) for memory development.

Selected Invited Talks: (from 75 invited talks)

1. *International Symposium on Materials for Enabling Nanodevices (ISMEN)*, UCLA, CA (2010). **(Plenary)**
2. *The 11th Non-Volatile Memory Technology Symposium (NVMTS)*, Shanghai, China (2011). **(Keynote)**
3. *The 224th Electrochemical Society Meeting, ULSI Process Integration Symposium.*, CA (2013). **(Keynote)**
4. *Special Lecture, AirForce Research Lab*, Rome, NY (2013). **(Chief Scientist Lecture Series)**

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5. *The IEEE International Symposium on Circuits and Systems (ISCAS), FEST 2014, Australia. (Keynote)*
 6. *Advances in ReRAM : Materials and Interfaces 2015, Crete, Greece. (Keynote)*
 7. *China Semiconductor Technology International Conference (CSTIC 2016), Shanghai, China (2016) (Keynote)*
 8. *International Workshop on Information Storage/10th International Symposium on Optical Storage (IWIS/ISOS 2016), Changzhou, China. (Keynote)*
 9. *International Conference on Memristive Materials, Devices & Systems (MEMRISYS) 2017, Athens, Greece (2017). (Plenary)*
 10. *China Semiconductor Technology International Conference (CSTIC2017), Shanghai, China (2017) (Keynote)*
 11. *International Symposium on Memory Devices for Abundant Data Computing, Hongkong, (2017) (Plenary)*
 12. *MRS Spring meeting, 2014, 2017 (invited talk); MRS Fall meetings, 2014, 2015, 2016, 2017 (Invited talks)*
 13. *International Conference on Memristive Materials, Devices & Systems (MEMRISYS) 2018, Beijing, China (2018). (Keynote)*
 14. *Nature Conference on Flexible Electronics-Visions of a Flexible Future, Xi'an, China (2018). (Keynote)*
 15. *The 3rd International Conference on New Material and Chemical Industry (NMC12018), Sanya, China (2018). (Keynote)*
 16. *The 6th Memristor and Memristive Symposium, Budapest, Hungary (2018). (plenary)*
 17. *International Emergent Memory Symposium (IEMS-2018), 2018, Ji'an, China. (plenary)*
 18. *International Conference on Neuromorphic Systems (ICONS-2018) Knoxville (2018), TN. (plenary)*

Academic Activities:

Associate Editors: *APPLIED PHYSICS A*: a research journal from Springer

Editorial Board: *SCIENTIFIC REPORTS*

Advisory Board:

ADVANCED MATERIALS TECHNOLOGIES: Editorial Advisory Board

Conference Chairs: The 8th and 10th IEEE Nanotechnology Symposia on “Emerging Non-volatile Memory Technologies” 2012, and “2D Devices and Materials” 2014, respectively;

Conference co-Chair: “The 1st IEEE Neuromorphic computing”, Sept. 2017.

Symposium co-chairs:

1. “Non-volatile Memory” in The IEEE International Electron Devices Meeting (IEDM) 2014;
2. "memristors" in the Electrochemical Society (ECS) Meeting, 2017;
3. “Ionics of memrsitor/resistive switches” in 21st Solid State Ionics (SSI), 2017;
4. “Memristive devices - from fundamentals to applications” in International Materials Research Congress (IMRC), 2017;
5. “Emerging Materials, Technologies and Applications for Non-volatile Memory Devices” in CIMTEC 2018.

Program/technical committees:

1. The EMN Meeting on Surface and Interface, 2016
2. The IEEE International Electron Devices Meeting (IEDM), 2014, 2015.

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3. 5th International Conference on Smart and Multifunctional Materials, Devices, Structures in CIMTEC 2016. (International Advisory Board)
 4. The IEEE Silicon Nanoelectronics Workshop (SNW) 2014
 5. The IEEE Non-Volatile Memory Technology Symposium (NVMTS). 2011-2017
 6. The International Conference on Advances in Circuits, Electronics and Micro-electronics, 2018.
 7. Elected officer, The IEEE Nanotechnology Council (SF and Bayarea) 2011-2014

Guest Editors:

- “Non-volatile memory based on nanostructures” (*NANOTECHNOLOGY* special issue, 2011);
- “Memristive and resistive devices and systems” (*APPLIED PHYSICS A* Special Issue, 2011);
- “Solid-state Memristive Devices and Systems” (IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2015)
- “Flexible Hybrid Electronics” (IEEE Access special issue, 2017)
- “Memresistive devices and their applications: Technology, Design, Automation and Computing” (IEEE Transaction on VLSI Special issue, 2017)
- “Memresistive devices and their applications: Technology, Design, Automation and Computing” (IEEE Transaction on VLSI Special issue, 2017)
- “Memristive Materials and Devices” (ADVANCED ELECTRONIC MATERIALS special issue, 2018)

**Detailed list of >130 refereed papers, 94 Granted Patents and >90 invited talks
by J. Joshua Yang**

Peer-reviewed papers (* indicates corresponding author):

Papers after joining UMass:

Journal papers

1. Z. Wang, M. Rao, J.-W. Han, J. Zhang, P. Lin, Y. Li, C. Li, W. Song, S. Asapu, R. Midya, Y. Zhuo, H. Jiang, J. H. Yoon, N. K. Upadhyay, S. Joshi, M. Hu, J. P. Strachan, M. Barnell, Q. Wu, H. Wu, Q. Qiu, R. S. Williams, Q. Xia*, and **J. Joshua Yang***, “Capacitive neural network with neuro-transistors”, *NATURE COMMUNICATIONS* **9**, 3208 (2018).
2. C. Li, D. Belkin, Y. Li, P. Yan, M. Hu, N. Ge, H. Jiang, E. Montgomery, P. Lin, Z. Wang, J. P. Strachan, M. Barnell, Q. Wu, R. S. Williams, **J. Joshua Yang***, and Q. Xia*, “Efficient and self-adaptive in-situ learning in multilayer memristive neural networks”, *NATURE COMMUNICATIONS* **9**, 2385 (2018).
3. Z. Wang, S. Joshi, S. Savel’ev, W. Song, R. Midya, Y. Li, M. Rao, P. Yan, S. Asapu, Y. Zhuo, H. Jiang, P. Lin, C. Li, J. H. Yoon, N. K. Upadhyay, J. Zhang, M. Hu, J. P. Strachan, M. Barnell, Q. Wu, H. Wu, R. Stanley Williams, Q. Xia, and **J. Joshua Yang***, “Fully memristive neural networks for inference and unsupervised learning”, *NATURE ELECTRONICS* **1**, 137-145 (2018).
4. C. Li, M. Hu, Y. Li, H. Jiang, N. Ge, E. Montgomery, Z. Li, J. P. Strachan*, P. Lin, W. Song, Z. Wang, M. Barnell, Q. Wu, R. S. Williams, **J. Joshua Yang***, Q. Xia*, “Analogue signal and image processing with large memristor crossbars”, *NATURE ELECTRONICS* **1**, 52-59 (2018).
5. M. Hu, C. E. Graves, C. Li, Y. Li, N. Ge, E. Montgomery, N. Davila, H. Jiang, R. S. Williams, **J. Joshua Yang***, Qiangfei Xia*, and John Paul Strachan*, “Memristor-based analog computation and neural network classification with a dot product engine”, *ADVANCED MATERIALS* **29**, 1705914 (2018).
6. J. H. Yoon, Z. Wang, K. M. Kim, H. Wu, V. Ravichandran, Q. Xia*, C. S. Hwang and **J. Joshua Yang***, “An Artificial Nociceptor Based on a Diffusive Memristor”, *NATURE COMMUNICATIONS* **8**, 417 (2018).
7. M. Wang, S. Cai, C. Pan, C. Wang, X. Lian, K. Xu, Y. Zhuo, **J. Joshua Yang***, P. Wang*, F. Miao*, “Ultra-robust memristors based on fully layered two-dimensional materials”, *NATURE ELECTRONICS* **1**, 130-136 (2018).
8. Z. Wang, M. Rao, R. Midya, S. Joshi, H. Jiang, P. Lin, W. Song, S. Asapu, Y. Zhuo, C. Li, H. Wu*, Q. Xia*, and **J. Joshua Yang***, “Threshold Switching of Ag or Cu in dielectrics: Materials, Mechanism, and Applications”, *ADVANCED FUNCTIONAL MATERIALS* **28**, 1704862 (invited feature article, 2018).
9. **J. Joshua Yang*** and Q. Xia, “Battery-like artificial synapses”, *NATURE MATERIALS* **16**, 396-397 (2017).
10. Z. Wang, S. Joshi, S. E. Savel’ev, H. Jiang, R. Midya, P. Lin, M. Hu, N. Ge, J. P. Strachan, Z. Li, Q. Wu, M. Barnell, G-L Li, H. L. Xin, R. S. Williams, Q. Xia, and **J. Joshua Yang***, “Memristors with diffusive dynamics as synaptic emulators for neuromorphic computing”, *NATURE MATERIALS* **16**, 101-108 (2017).
11. R. Midya, Z. Wang, J. Zhang, C. Li, S. Joshi, H. Jiang, P. Lin, K. Norris, N. Ge, Q. Wu, M. Barnell, Z. Li, R. S. Williams, Q. Xia*, and **J. Joshua Yang***, “Anatomy of Ag/hafnia based selectors with 10^{10} nonlinearity”, *ADVANCED MATERIALS* **29**, 1604457 (2017).
12. J. H. Yoon, J. Zhang, X. Ren, Z. Wang, H. Wu, Z. Li, M. Barnell, Q. Wu, L. J. Lauhon, Q. Xia and **J. Joshua Yang***, “Truly Electroforming-Free and low- Energy

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- Memristors with Pre-conditioned Conductive Tunneling Paths”, *ADVANCED FUNCTIONAL MATERIALS* **27**, 1702010 (2017).
13. H. Jiang, D. Belkin, S. Savel'ev, S. Lin, Z. Wang, Y. Li, S. Joshi, R. Midya, C. Li, M. Rao, M. Barnell, Q. Wu, **J. Joshua Yang**^{*}, Q. Xia^{*}, “A novel true random number generator based on a stochastic diffusive memristor”, *NATURE COMMUNICATIONS* **8**, 882 (2017).
 14. R. Zhang, W. Pang, Z. Feng, X. Chen, Y. Chen, Q. Zhang, H. Zhang, C. Sun, **J. Joshua Yang**, and Da. Zhang. "Enabling selectivity and fast recovery of ZnO nanowire gas sensors through resistive switching." *SENSORS AND ACTUATORS B: CHEMICAL* **238**, 357-363 (2017).
 15. J. J. Diaz Leon, K. J. Norris, **J. Joshua Yang**, J. F. Sevic, N. P. Kobayashi, “A niobium oxide-tantalum oxide selector-memristor self-aligned nanostack”, *APPLIED PHYSICS LETTERS* **110**, 103102 (2017).
 16. X. Lian, M. Wang, P. Yan, **J. Joshua Yang**^{*}, F. Miao, “Reset switching statistics of TaO_x-based Memristor”, *JOURNAL OF ELECTROCERAMICS*, <https://doi.org/10.1007/s10832-017-0094-x> (2017).
 17. C. Li, L. Han, H. Jiang, M. Jang, **J. Joshua Yang**, H. L. Xin and Q. Xia, “3-Dimensional Crossbar Arrays of Self-rectifying Si/SiO₂/Si Memristors”, *NATURE COMMUNICATIONS* **8**, 15666 (2017).
 18. X. Lian, M. Wang, M. Rao, P. Yan, **J. Joshua Yang**^{*}, F. Miao, “Characteristics and transport mechanisms of multiple triple resistance switching regimes of TaO_x memristor”, *APPLIED PHYSICS LETTERS*, **110**, 173504 (2017).
 19. M. Hu, Y. Chen, Y. Wang, H. H. Li, “A Compact Memristor-Based Dynamic Synapse for Spiking Neural Networks”, *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS* **8**, 1353 (2017).
 20. Ch. Wu, T. W. Kim, H. Y. Choi, D. U. Lee, D. R. Strukov and **J. Joshua Yang**, “flexible 3D artificial synapse networks with correlated learning and trainable memory capability”, *NATURE COMMUNICATIONS* **8**, 752 (2017).
 21. Ch. Wu, T. W. Kim, T. Guo, F. Li, D. U. Lee, and **J. Joshua Yang**, “Mimicking classical conditioning based on a single flexible memristor”, *ADVANCED MATERIALS* **29**, 1602890 (2017).
 22. Z. Wang, H. Jiang, M. Jang, P. Lin, A. Ribbe, Qing Wu, Mark Barnell, Qiangfei Xia, and **J. Joshua Yang**^{*} "Electrochemical Metallization Switching with a Platinum Group Metal in Different Oxides", *NANOSCALE* **8**, 14023-14030 (2016).
 23. B. J. Choi, J. Zhang, K. Norris, G. Gibson, K. M. Kim, W. Jackson, M. Zhang, Z. Li, **J. Joshua Yang**^{*}, and R. Stanley Williams^{*}, “Trilayer Tunnel Selectors for Memristor Memory Cells”, *ADVANCED MATERIALS* **28**, 356-362 (2016).
 24. B. J. Choi, A. C. Torrezan, J. P. Strachan, P. G. Kotula, A. J. Lohn, M. J. Marinella, R. S. Williams^{*} and **J. Joshua Yang**^{*}, “High-speed and low-energy nitride memristors”, *ADVANCED FUNCTIONAL MATERIALS* **26**, 5290-6296 (2016).
 25. W. Yi, S. E. Savel'ev, G. Medeiros-Ribeiro, F. Miao, M.-X. Zhang, **J. Joshua Yang**, A. M. Bratkovsky, and R. S. Williams, “Enhanced noise at quantum conductance in memristors”, *NATURE COMMUNICATIONS* **7**, 11142 (2016).
 26. K. M. Kim, **J. Joshua Yang**, J. P. Strachan, E. M. Grafals, N. Ge, N. D. Melendez, Z. Li, and R. S. Williams, “Voltage divider effect for the improvement of variability and endurance of TaO_x memristor”, *SCIENTIFIC REPORTS* **6**, 20085- (2016).
 27. X. Liu, M. Mao, B. Liu, B. Li, Y. Wang, H. Jiang, M. Barnell, Q. Wu, **J. Joshua Yang**, H. Li, Y. Chen, “Harmonica: A Framework of Heterogeneous Computing

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- Systems with Memristor-based Neuromorphic Computing Accelerators”, *IEEE TRANSACTIONS ON CAS I* **63.5**, 617 (2016).
28. H. Jiang, L. Han, P. Lin, Z. Wang, M. H. Jang, **J. Joshua Yang**, H. Xin, and Q. Xia, “Sub-10 nm Ta channel responsible for superior performance of a HfO₂ memristor”, *SCIENTIFIC REPORTS* **6**, 28525 (2016).
 29. J. Zhang, K. J. Norris, G. Gibson, D. Zhao, K. Samuels, M. Zhang, **J. Joshua Yang**, J. Park, R. Sinclair, Y. Jeon, Z. Li, R. S. Williams, “Thermally induced crystallization in NbO₂ thin films”, *SCIENTIFIC REPORTS* **6**, 34294 (2016).
 30. N. K. Upadhyay, J. Saamil, and **J. Joshua Yang***, “Synaptic electronics and neuromorphic computing”, *SCIENCE CHINA INFORMATION SCIENCES* **59**, 061404 (2016).
 31. M. Hu, Y. Chen, **J. Joshua Yang**, Y. Wang, H. Li, “A Memristor-based Dynamic Synapse for Spiking Neural Networks” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 10.1109/TCAD.2016.2618866 (2016).
 32. R. Zhang, W. Pang, Q. Zhang, Y. Chen, X. Chen, Z. Feng, **J. Joshua Yang**, and D. Zhang. "Enhanced non-volatile resistive switching in suspended single-crystalline ZnO nanowire with controllable multiple states." *NANOTECHNOLOGY* **27**, 315203 (2016).
 33. K. M. Kim, J. Zhang, C. Graves, **J. Joshua Yang**, B. J. Choi, C. S. Hwang, Z. Li, R. S. Williams, “Low power, self-rectifying, and forming-free memristor with an asymmetric programming voltage for a high density crossbar application”, *NANO LETTERS* **16**, 6724-6732 (2016).
 34. N. Ge*, J. H. Yoon, M. Hu, E. J. Merced-Grafals, Z. Li, H. Holder, Q. Xia, R. S. Williams, X. Zhou, **J. Joshua Yang***, “An efficient analog Hamming distance comparator based on a diagonal memristive crossbar array” *SCIENTIFIC REPORTS* **7**, 40135 (2016).
 35. L. Zhang, N. Ge, **J. Joshua Yang**, Z. Li, R. S. Williams, and Y. Chen, “Low voltage two-state-variable memristor model of vacancy-drift resistive switches”, *APPLIED PHYSICS A* **119**, 1-9 (2015).
 36. M. Wang, X. Lian, Y. Pan, B. Wang, **J. Joshua Yang***, F. Miao, and D. Xing, “A selector device based on graphene-oxide heterostructures for memristor crossbar applications”, *APPLIED PHYSICS A* **120**, 403-407 (2015).
 37. K. M. Kim, **J. Joshua Yang**, E. Merced, C. Graves, S. Lam, N. Davila, M. Hu, N. Ge, Z. Li, R. S. Williams, and C. S. Hwang, “Low Variability Resistor–Memristor Circuit Masking the Actual Memristor States”, *ADVANCED ELECTRONIC MATERIALS* **1**, 1500095 (2015).
 38. J. Zhang, K. Norris, K. Samuels, N. Ge, M. Zhang, J. Park, R. Sinclair, G. Gibson, **J. Joshua Yang**, Z. Li and R. S. Williams, “Electron Energy-Loss Spectroscopy (EELS) Study of NbO_x Film for Resistive Memory Applications”, *MICROSCOPY AND MICROANALYSIS* **21**, 285 (2015).
 39. R. Zhang, H. Jiang, Z. Wang, P. Lin, Ye. Zhuo, D. Holcomb, D. Zhang, **J. Joshua Yang**, Q. Xia, “Nanoscale Diffusive Memristor Crossbars as Physical Unclonable Functions”, *NANOSCALE* **10**, 2721, (2018).
 40. T. Ahmed, S. Walia, E. L.H. Mayes, R. Ramanathan, P. Guagliardo, V. Bansal, M. Bhaskaran, **J. Joshua Yang**, S. Sriram, “Inducing tunable switching behavior in a single memristor”, *APPLIED MATERIALS TODAY* **11**, 280-290 (2018).
 41. L. Zhang, W. Song, **J. Joshua Yang**, H. Li, Y. Chen, “A compact model for selectors based on diffusive memristors”, *APPLIED PHYSICS A* **124**, 333 (2018).

Journal papers (currently under revision):

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4. United States Patent, US8,093,575, 2011, "Memristive device with a bi-metallic electrode", Q. Xia, X. Li, **J. Joshua Yang**.
5. United States Patent, US8,063,395, 2011, "Memristor amorphous metal alloy electrodes", Q. Xia, **J. Joshua Yang**, S. Y. Wang.
6. United States Patent US8,207,593, 2012, "Memristor having a nanostructure in the switching material" A. M. Bratkovski, **J. Joshua Yang**, Q. Xia.
7. United States Patent US8,203,171, 2012, "Defective graphene-based memristor" **J. Joshua Yang**, F. Miao, W. Wu, S.-Y. Wang, R. S. Williams.
8. United States Patent US8,207,520, 2012, "Programmable crosspoint device with an integral diode" **J. Joshua Yang**, G. M. Ribeiro, R. S. Williams.
9. United States Patent US8,283,649, 2012, "Memristor with a non-planar substrate" A. M. Bratkovski, S.-Y. Wang, **J. Joshua Yang**, M. Stuke.
10. United States Patent US8,264,868, 2012, "Memory array with metal-insulator transition switching devices" G. M. Ribeiro, Pickett, Matthew, **J. Joshua Yang**.
11. United States Patent US8,259,485, 2012, "Multilayer structures having memory elements with varied resistance of switching layers" **J. Joshua Yang**, J. P. Strachan, W. Wu.
12. United States Patent US8,294,132, 2012, "Graphene memristor having modulated graphene interlayer conduction" F. Miao, **J. Joshua Yang**, W. Wu, S.-Y. Wang, R. S. Williams.
13. United States Patent US8,226,3521, 2012, "Memristors with an electrode metal reservoir for dopants" **J. Joshua Yang**, W. Yi, M. Stuke, S.-Y. Wang.
14. United States Patent US8,225,8304, 2012, "Guided mode resonator based raman enhancement apparatus" W. Wu, Q. Xia, J. Li, **J. Joshua Yang**.
15. United States Patent US8,226,4724, 2012, "Changing a memristor state" F. Miao, **J. Joshua Yang**, G. M. Ribeiro, R. S. Williams.
16. United States Patent USPTO US8,324,976 B2, 2012, "Oscillator circuitry having negative differential resistance" J. Borghetti, M. D. Pickett, G. Medelros-Ribeiro, W. Yi, **J. Joshua Yang**, M. Zhang.
17. United States Patent US8,385,101, 2013, "Memory resistor having plural different active materials" **J. Joshua Yang**, M. Zhang, R. S. Williams.
18. United States Patent USPTO US8,415,652, 2013, "Memristors with a switching layer comprising a composite of multiple phases" **J. Joshua Yang**, G. M. Ribeiro, R. S. Williams.
19. United States Patent USPTO US8,437,172, 2013, "Decoders using memristive switches" M. Fiorentino, W. M. Tong, P. J. Kuekes, **J. Joshua Yang**.
20. United States Patent USPTO US8,437,072, 2013, "Individually addressable nano mechanical actuator and contact switch by redox reaction in a crossbar array" **J. Joshua Yang**, R. S. Williams, W. M. Tong.
21. United States Patent USPTO US8,450,711, 2013, "Semiconductor memristor devices" R. S. Williams, **J. Joshua Yang**, D. R. Stewart.
22. United States Patent USPTO US8,455,852, 2013, "Controlled placement of dopants in memristor active regions" N. J. Quitoriano, P. J. Kuekes, **J. Joshua Yang**.
23. United States Patent USPTO US8,487,289, 2013, "Electrically actuated device" **J. Joshua Yang**, M. Zhang, G. Medelros-Ribeiro.

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24. United States Patent USPTO US 8,525,146, 2013, "Electrical circuit component" W. Wu, M. D. Pickett, **J. Joshua Yang**, Q. Xia, G. Medeiros Ribeiro.
 25. United States Patent USPTO US8,525,553, 2013, "Negative differential resistance comparator circuits" M. D. Pickett, **J. Joshua Yang**, M. Zhang.
 26. United States Patent USPTO US8,519,372, 2013, "Electroforming-free nanoscale switching device" **J. Joshua Yang**, S.-Y. Wang, R. S. Williams, A. Bratkovski, G. Medeiros Ribeiro.
 27. United States Patent USPTO US8,530,873, 2013, "Electroforming free memristor and method for fabricating thereof" **J. Joshua Yang**, G. Medeiros Ribeiro, R. S. Williams.
 28. United States Patent USPTO US8,546,785, 2013, "Memristive device" **J. Joshua Yang**, F. Miao, W. Wu, S.-Y. Wang, R. S. Williams.
 29. United States Patent USPTO US8,575,585, 2013, "Memristive device" **J. Joshua Yang**, Q. Xia, A. A. Bratkovski.
 30. United States Patent USPTO US8,570,138, 2013, "Resistive Switches" **J. Joshua Yang**, D. B. Strukov, S. Y. Wang.
 31. United States Patent USPTO US8,586,959, 2013, "Memristive switch device" M. D. Pickett, **J. Joshua Yang**, D. B. Strukov.
 32. United States Patent USPTO US8,587,985, 2013, "Memory array with graded resistance lines" **J. Joshua Yang**, J. P. Strachan, W. Wu, Janice H. Nickel.
 33. United States Patent USPTO US8,710,483 B2, 2014, "Memristive junction with intrinsic rectifier" J. Joshua Yang, J. P. Strachan, M. D. Pickett.
 34. United States Patent USPTO US8,710,865, 2014, "Field-programmable analog array with memristors" **J. Joshua Yang**, M. S. Qureshi, G. Medeiros-Ribeiro, R. S. Williams.
 35. United States Patent USPTO US8,711,594, 2014, "Asymmetric switching rectifier" M.-X. Zhang, **J. Joshua Yang**, R. S. Williams.
 36. United States Patent USPTO US8,737,113, 2014, "Memory resistor having multi-layer electrodes" **J. Joshua Yang**, W. Wu, R. Gilberto-Ribeiro.
 37. United States Patent USPTO US9,018,083 B2, 2014, "Electrically actuated device and method of controlling the formation of dopants therein" **J. Joshua Yang**, D. Stewart, P. J. Kuekes, W. M. Tong.
 38. United States Patent USPTO US8,767,438, 2014, "Memelectronic Device" **J. Joshua Yang**, B. J. Choi, M. -X. Max Zhang, G. Medeiros-Ribeiro, R. S. Williams.
 39. United States Patent USPTO US8,766,231, 2014, "Nanoscale Electronic Device with Barrier Layers" Wei Yi, **J. Joshua Yang**, G. Medeiros-Ribeiro.
 40. United States Patent USPTO US8,779,409, 2014, "Low energy memristors with engineered switching channel materials" **J. Joshua Yang**, M.-X. Zhang, G. Medeiros-Ribeiro, R. S. Williams.
 41. United States Patent USPTO US8,779,848, 2014, "Two terminal memcapacitor device" M. D. Pickett, J. Borghetti, **J. Joshua Yang**.
 42. United States Patent USPTO US8,891,284, 2014, "Memristors based on mixed-metal-valence compounds" R. S. Williams, **J. Joshua Yang**, M. D. Pickett, G. Medeiros-Ribeiro, J. P. Strachan.
 43. United States Patent USPTO US8,809,158, 2014, "Device having memristive memory" M. D. Pickett, **J. Joshua Yang**, G. Medeiros-Ribeiro.
 44. United States Patent USPTO US8,829,581, 2014, "Resistive memory devices" S. Y. Wang, **J. Joshua Yang**, A. A. Bratkovski, R. S. Williams.
 45. United States Patent USPTO US8,923,034, 2014, "Multi-level memory cell with continuously tunable switching" Y. Wei, F. Miao, **J. Joshua Yang**.
 46. United States Patent USPTO US8,872,153, 2014, "Device structure for long endurance memristors" **J. Joshua Yang**, M.-X. Zhang, R.S. Williams.
 47. United States Patent USPTO US8,882,217, 2014, "Printhead assembly including memory elements" P. V. Lea, G. M. Ribeiro, M. D. Pickett, **J. Joshua Yang**.
 48. United States Patent USPTO US8,879,300, 2014, "Switchable two-terminal devices with diffusion/drift species" **J. Joshua Yang**, W. Wu, Q. Xia.

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49. United States Patent USPTO US8,878,342, 2014, "Using alloy electrodes to dope memristors" N. J. Quitoriano, D. Ohlberg, P. J. Kuekes, **J. Joshua Yang**.
 50. United States Patent USPTO US8,890,106, 2014, "Hybrid circuit of nitride-based transistor and memristor" **J. Joshua Yang**, G. Medeiros-Ribeiro, B. J. Choi, R. S. Williams.
 51. United States Patent USPTO US8,912,520, 2014, "Nanoscale switching device" **J. Joshua Yang**, M. D. Pickett, G. Medeiros-Ribeiro.
 52. United States Patent USPTO US8,921,960, 2015, "Memristor cell structures for high density arrays" **J. Joshua Yang**, M. X. Zhang, G. Medeiros-Ribeiro, R. S. Williams.
 53. United States Patent USPTO US9,082,533, 2015, "Memristive element based on hetero-junction oxide" **J. Joshua Yang**, M. X. Zhang, R. S. Williams.
 54. United States Patent USPTO US9,159,476 B2, 2015, "Negative differential resistance device" **J. Joshua Yang**, M. X. Zhang, R. S. Williams.
 55. United States Patent USPTO US9,000,411 B2, 2015, "Memristor devices configured to control bubble formation" Z. Li, A. M. Bratkovski, **J. Joshua Yang**.
 56. United States Patent USPTO US8,766,228, 2014, "Electrically actuated device and method of controlling the formation of dopants therein" **J. Joshua Yang**, D. R. Stewart, P. J. Kuekes, W. M. Tong.
 57. United States Patent USPTO US9,024,285, 2015, "Nanoscale switching devices with partially oxidized electrodes" **J. Joshua Yang**, G. M. Ribeiro, R. S. Williams.
 58. United States Patent USPTO US9,466,793, B2, 2015, "Memristors having at least one junction" H. S. Cho, **J. Joshua Yang**, J. H. Nickel.
 59. United States Patent USPTO US9,041,157, B2, "Method for doping an electrically actuated device" W. Wu, S. V. Mathai, S.-Y. Wang, **J. Joshua Yang**.
 60. United States Patent USPTO US9,040,285 B2, 2015, "Nanoscale switching device" G. Medeiros-Ribeiro, J. H. Nickel, **J. Joshua Yang**.
 61. United States Patent USPTO US9,082,972 B2, 2015, "Bipolar resistive switch heat mitigation" J. P. Strachan, G. Medeiros Ribeiro, **J. Joshua Yang**, W. Yi.
 62. United States Patent USPTO US9,196,354, 2015, "Memory resistor adjustment using feedback control" J. P. Strachan, J. Borghetti, M. D. Pickett, G. Ribeiro, **J. Joshua Yang**.
 63. United States Patent USPTO US9,184,213, 2015, "Nanoscale switching device" **J. Joshua Yang**, D. B. Strukov, W. Wu.
 64. United States Patent USPTO US9,184,382, 2015, "Memristive devices with layered junctions and methods for fabricating the same" M. D. Pickett, **J. Joshua Yang**, G. Medeiros-Ribeiro.
 65. United States Patent USPTO US9,178,153, 2015, "Memristor structure with a dopant source" M. X. Zhang, **J. Joshua Yang**, R. S. Williams.
 66. United States Patent USPTO US9,171,613, 2015, "Memristors with asymmetric electrodes" A. M. Bratkovski, **J. Joshua Yang**, S.-Y. Wang, M. Stuke.
 67. United States Patent USPTO US9,165,645, 2015, "High-reliability high-speed memristor" F. Miao, **J. Joshua Yang**, J. P. Strachan, W. Yi, G. Medeiros-Ribeiro, R. S. Williams.
 68. United States Patent USPTO US8,982,601 B2, 2015, "Switchable junction with an intrinsic diode formed with a voltage dependent resistor" **J. Joshua Yang**, J. P. Strachan, J. Borghetti, M. D. Pickett.
 69. United States Patent USPTO US9,224,949 B2, 2015, "Memristive elements that exhibit minimal sneak path current" **J. Joshua Yang**, M. X. Zhang, R. S. Williams.
 70. United States Patent USPTO US9,257,645 B2, 2016, "Memristors having mixed oxide phases" **J. Joshua Yang**, M. X. Zhang, F. Miao.
 71. United States Patent USPTO US9,293,200 B2, 2016, "Multilayer memory array" J. H. Nickel, G. Medeiros-Ribeiro, **J. Joshua Yang**.
 72. United States Patent USPTO US9,331,278 B2, 2016, "Forming memristors on imaging devices" **J. Joshua Yang**, N. Ge, Z. Li, M. X. Zhang.
 73. United States Patent USPTO US9,276,204 B2, 2016, "Memristor with channel region in thermal equilibrium with containing region" F. Miao, **J. Joshua Yang**, J. P. Strachan, W. Yi, G. Medeiros Ribeiro, R. Stanley Williams.

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74. United States Patent USPTO US9,224,821 B2, 2015, “Customizable nonlinear electrical devices” M. X. Zhang, **J. Joshua Yang**, G. Medeiros Ribeiro, R. S. Williams.
 75. United States Patent USPTO US9,478,738 B2, 2016, “High-reliability high-speed memristor” F. Miao, **J. Joshua Yang**, J. P. Strachan, W. Yi, G. Medeiros Ribeiro, R. S. Williams.
 76. United States Patent USPTO US9,508,928 B2, 2016, “Nanochannel array of nanowires for resistive memory devices” S.-Y. Wang, **J. Joshua Yang**.
 77. United States Patent USPTO US9,558,869, 2017, “Negative differential resistance device” **J. Joshua Yang**, M. Zhang, R. S. Williams.
 78. United States Patent USPTO US9,847,124, B2, 2017, “Resistive elements to operate as a matrix of probabilities”, M. Hu, J. P. Strachan, G. Ning, **J. Joshua Yang**.
 79. United States Patent USPTO US9,847,378, B2, 2017, “Resistive memory devices with a multi-component electrode” X. Sheng, Y. Jeon, **J. Joshua Yang**, H. S. Cho, R. H. Henze.
 80. United States Patent USPTO US9,776,400, B2, 2017, “Printhead with a number of memristor cells and a parallel current distributor” N. Ge, **J. Joshua Yang**, Z. Li.
 81. United States Patent USPTO US9,701,115, B2, 2017, “Printheads having memories formed thereon” **J. Joshua Yang**, N. Ge, Z. Li.
 82. United States Patent USPTO US9, 793,322, B2, 2017, “Apparatus having first and second switching materials” N. Ge, **J. Joshua Yang**, R. S. Williams, K. M. Kim.
 83. United States Patent USPTO US9,793,473, B2, 2017 “Memristor structures” S. Y. Wang, **J. Joshua Yang**, M. M. Zhang, A. M. Bratkovski.
 84. United States Patent USPTO US9,885,937, B2, 2018, “Dynamical optical crossbar array” **J. Joshua Yang**, A. M. Bratkovski, D. A. Fattal, M. Zhang.
 85. United States Patent USPTO US9,870,822, B2, 2018, “Non-volatile memory element with thermal-assisted switching control” G. Ning, **J. Joshua Yang**, Z. Li.
 86. United States Patent USPTO US9,947,405, B2, 2018 “Memristive dot product engine with a nulling amplifier” J. P. Strachan, G. E. Montgomery, N. Ge, M. Hu, **J. Joshua Yang**.
 87. United States Patent USPTO US9,911,789, B2, 2018 “1-Selector n-Resistor memristive devices” **J. Joshua Yang**, G. Gibson, Z. Li.
 88. United States Patent USPTO US9,911,490, B2, 2018 “Memory controllers” N. Ge, **J. Joshua Yang**, F. Perner, J. H. Nickel.
 89. United States Patent USPTO US9, 889,659, B2, 2018 “Printhead with a memristor” N. Ge, **J. Joshua Yang**, M. Zhang.
 90. United States Patent USPTO US9,934,852 B2, 2018 “Sensing an output signal in a crossbar array based on a time delay between arrival of a target output and a sneak output” K. M. Kim, N. Ge, **J. Joshua Yang**.
 91. United States Patent USPTO US9, 911,915 B2, 2018 “Multiphase selectors” **J. Joshua Yang**, Y. Jeon, H. S. Cho.
 92. United States Patent USPTO US9,934,849 B2, 2018 “Asymmetrically selecting memory elements” K. M. Kim, **J. Joshua Yang**, Z. Li.
 93. United States Patent USPTO US9, 911,788 B2, 2018 “Selectors with oxide-based layers” **J. Joshua Yang**, Ning Ge, Zhiyong Li.
 94. EP 2,842,163 B1, 2018 “Nonlinear memristors” **J. Joshua Yang**, M. Zhang, M. D. Pickett, R. S. Williams.

Invited/Plenary/Keynote Talks:

International conferences:

1. *The 10th Non-volatile memory technology symposium (NVMTS09)*, 2009, Portland, Oregon.
2. “Oxide based memristive nanodevices”, 2009, **International Conference on Communications, Circuits and Systems 2009 (ICCCAS 2009)** San Jose, California.
3. “Metal/oxide/metal memristive devices”, 2009, **The 7th International Conference on Advanced Materials and Devices (ICAMD 2009)**, Jeju island, KOREA.

4. "Engineering control and applications of oxide based nano-switches", 2010, **International Symposium on Integrated Functionalities (ISIF 2010)**, San Juan, Puerto Rico.
5. "Engineering control over device properties of memristors for immediate applications", 2010, **Julius Springer Forum on Applied Physics**, Stanford University, CA.
6. "Promises and challenges of Memristive switches", 2011, **11th Non-Volatile Memory Technology Symposium**, Shanghai, China. **(Keynote)**
7. "Oxide based memristive devices", 2012, **IEEE International Conference on Solid-State and Integrated Circuit Technology**, 2012, Xi'an, China.
8. "TaOx based memristive devices", 2012, **12th Non-Volatile Memory Technology Symposium**, Singapore.
9. "Memristive nanodevices for computing", 2013, **The 57th International Conference on Electron, Ion, Photon Beam Technology and Nanofabrication (EIPBN)**, Tennessee.
10. "Memristive Devices for Computing", 2013, **The 224th Electrochemical Society Meeting, ULSI Process Integration Symposium**, San Francisco, California. **(Keynote)**
11. "Memristive Nanodevices", *Nano and Giga 2014*, Phoenix, Arizona.
12. "Challenges and Materials Solutions for Memristive Devices (ReRAM)", **MRS Spring 2014**, San Francisco, California.
13. "The material perspective ReRAM" **The IEEE International Symposium on Circuits and Systems (ISCAS)**, FEST 2014, Melbourne, Australia. **(Keynote)**
14. "Tutorial on Memristive devices" **the 29th Symposium on on Microelectronics Technology and Devices, 2014 (SBMICRO 2014, Chip in Aracaju)**, Aracaju, Brazil.
15. "Challenges and solutions of memristors for Neuromorphic Computing" **the International Symposium on Neuromorphic Systems and Cyborg Intelligence**, 2014, Hangzhou, China.
16. "Materials Perspective of Memristive Devices", **IEEE International Conference on Solid-State and Integrated Circuit Technology**, 2014, Guilin, China.
17. "Challenges and Solutions for Memristive Devices", **The AVS 61st International Symposium & Exhibition**, 2014, Baltimore, Maryland.
18. "RRAM tutorial", **MRS Fall Meeting 2014**, Boston, Massachusetts.
19. "Memristive Devices (ReRAM): Challenges and Possible Solutions", **MRS Fall Meeting 2015**, Boston, Massachusetts.
20. "Promises and challenges of memristive devices", **15th INTERNATIONAL CONFERENCE ON NANOTECHNOLOGY (IEEE Nano 2015)** 2015, Rome, Italy.
21. "Memristive nanodevices for computing - challenges and solutions", **China Semiconductor Technology International Conference 2015 (IEEE CSTIC 2015)** 2015, Shanghai, China.
22. "Challenges and possible solutions for memristive devices", **15th Non-Volatile Memory Technology Symposium (IEEE NVMTS 2015)**, 2015 Beijing, China.
23. "Engineering interfaces for memristive devices", **the 43rd Conference on the Physics and Chemistry of Surfaces and Interfaces (PCSI-43)**, Palms Springs, CA, 2016.
24. "Materials issues in memristive devices", **145th TMS annual meeting, 2016**, Nashville, Tennessee.
25. "Different applications of memristors enabled by selector devices", **China Semiconductor Technology International Conference (CSTIC), 2016**, Shanghai, China. **(Keynote)**
26. **J. Joshua Yang**, "Memristor Mate devices", **International Workshop on Information Storage/10th International Symposium on Optical Storage (IWIS/ISOS 2016)**, Changzhou, China. **(Keynote)**
27. "A versatile two-terminal device enables different applications of resistance switches" **The IEEE International Symposium on Circuits and Systems (ISCAS)**, 2016, Montréal, Canada.
28. "Challenges and solutions for memristors used for memory and neuromorphic computing", **16th Non-Volatile Memory Technology Symposium (IEEE NVMTS 2016)**, 2016 Pittsburg, Pennsylvania.
29. "Engineered materials for memristor mate" **International Conferences on Modern Materials and Technologies (CIMTEC)**, 2016, Perugia, Italy.
30. "Engineered materials for memristor mate" **58th Electronic Materials Conference (EMC)**, 2016, Newark, Delaware.

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31. “non-volatile memories” **230th Meeting of Electrochemical Society (ECS)**, 2016, Honolulu, Hawaii.
 32. “Memristors with diffusive relaxation dynamics for neuromorphic computing”, **IEEE 13th International Conference on Solid-State and Integrated Circuit Technology (ICSICT), 2016**, Hangzhou, China.
 33. “memristors with diffusive relaxation dynamics for neuromorphic computing”, 2016, **16th Non-Volatile Memory Technology Symposium**, Pennsylvania, USA.
 34. “Emerging Materials and Technologies for Nonvolatile Memories”, **MRS Fall Meeting 2016**, Boston, Massachusetts.
 35. “Challenges and solutions for memristors used for memory and neuromorphic computing”, **MRS Spring Meeting 2017**, Phoenix, Arizona.
 36. “Challenges and solutions for memristors used for memory and neuromorphic computing”, **Collaborative Conference on Materials Research (CCMR)**, 2017, Jeju Island, South Korea.
 37. “Diffusive memristors for future computing”, **China Semiconductor Technology International Conference (CSTIC), 2017**, Shanghai, China. **(Keynote)**
 38. “Diffusive Memristors” **1st International Conference on Memristive Materials, Devices & Systems (MEMRISYS)**, Athens, Greece (2017). **(Plenary)**
 39. “Diffusive Memristors for Computing”, **The 21st International Conference on Solid State Ionics (SSI-21)**, 2017, Padua, Italy.
 40. “RRAM/memristor for computing” **International Symposium on Memory Devices for Abundant Data Computing**, Hongkong, (2017) **(Plenary)**.
 41. “Diffusive Memristors as Artificial Synapses and Neurons for Neural Networks”, **MRS Fall Meeting 2017**, Boston, Massachusetts.
 42. “Diffusive memristor as an oscillatory neuron for brain inspired computing”, **XXVI International Materials Research Congress 2017**, Cancun, Mexico.
 43. “Bio-inspired computing with memristive devices”, **Neurotalk 2018**, Bangkok, Thailand.
 44. “Neuromorphic computing with memristive devices and arrays”, **Compound Semiconductor Week (CSW2018)**, 2018, MIT, Cambridge, USA.
 45. “Diffusive memristor for computing”, **The IEEE International Symposium on Circuits and Systems (ISCAS)**, 2018, Florence, Italy.
 46. “Diffusive Memristors for computing”, **International Conference on Memristive Materials, Devices & Systems (MEMRISYS)**, 2018, Beijing, China.
 47. “Neuromorphic computing with memristors”, **Nature Conference on Flexible Electronics-Visions of a Flexible Future**, 2018, Xi'an, China. **(Keynote)**
 48. “Experimental demonstrations of unconventional computing with memristive devices”, **the International Conference on Neuromorphic Systems**, 2018, Knoxville, Tennessee.
 49. “Memristive materials and applications”, **The 3rd International Conference on New Material and Chemical Industry (NMCI2018)**, Sanya, China (2018). **(Keynote)**
 50. “Unconventional computing with memristive devices and arrays” **AiMES 2018**, Cancun, Mexico.
 51. “Unconventional computing with memristive neural network”, **China Semiconductor Technology International Conference (CSTIC), 2018**, Shanghai, China.
 52. “Unconventional computing with memristive devices and arrays” **ACS Presidential Symposium**, 256th ACS National Meeting, Boston, MA.
 53. “Diffusive memristor for computing”, **The 6th Memristor and Memristive Symposium**, Budapest, Hungary (2018). **(plenary)**
 54. “Unconventional computing with resistive switching devices”, **International Emergent Memory Symposium (IEMS-2018)**, 2018, Ji'an, China. **(plenary)**

International workshops:

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55. The memristor at age 40”, 2010, **International Symposium on Materials for Enabling Nanodevices**, UCLA, California. (**Plenary talk**)
 56. “Applications and property engineering of memristive nanodevices”, 2010, **Advances in nonvolatile memory materials and devices**, *Suzhou*, China.
 57. “Recent progress on oxide based memristive devices in HP”, 2011, **Non-volatile memories workshop**, University of California - San Diego, California.
 58. “Oxide based memristive devices”, 2011, **Frontier of Functional-Oxide Nano Electronics workshop**, Tsukuba, Japan.
 59. “TaOx Memristive Nano-devices: Mechanism, Applications and Challenges”, 2012, **Advanced Memory Workshop**, NCCAUS Thin Film Users Group, California.
 60. “The Memristor” *LASERION international workshop*, 2013, Munich, Germany.
 61. “Memristive Devices for Computing” **Global Forum on Nanoelectronic Manufacturing: From Materials to Systems**, 2014 Mumbai, India.
 62. “Memristive nanodevices for computing - challenges and solutions”, **International workshop Advances in ReRAM: Materials and Interfaces 2015**, Crete, Greece. (**Keynote**)
 63. “Experimental demonstration of analog computing and neuromorphic computing with memristor crossbar arrays” **Energy Consequences of Information Workshop**, 2017 Santa Fe, New Mexico.
 64. “Unconventional computing using neural network based memristors”, 2017, **The 2017 Stephen and Sharon Seiden Frontiers in Engineering & Science Workshop: “Beyond CMOS: From Devices to Systems”**, Haifa, Israel.
 65. “Memristive devices for neuromorphic computing”, **the 2017 APS/CNM Users Meeting**, 2017, Argonne National Labs, Illinois.
 66. “Experimental demonstration of analog computing and neuromorphic computing with memristor crossbar arrays”, **2017 Energy Consequences of Information (ECI)**, 2017, Santa Fe, NM.
 67. “Diffusive Memristor based Neural Networks”, 2017, **International Workshop on Future Computing (IWofC)**, Beijing, China.
 68. “Challenges and possible solutions for RRAM based computing”, 2017, **the 7th International Workshop on Resistive Switching Memory**, Leuven, Belgium.
 69. “Opportunities and Challenges of Memristive Electroceramics for Computing”, 2017, **Frontiers In Electroceramics Workshop**, MIT, Massachusetts.
 70. “Resistive/memristive switching devices for computing”, 2017, **IEEE-IRDS Beyond CMOS Workshop**, Albuquerque, NM.

Seminars:

71. “Resistance Memory Nanoelectronics”, May/2009, *Invited Lecture*, **UCSC-NASA Ames Research Center**, Mountain View, California.
72. “Oxide based memristive junctions: switching, forming and device family”, 2009, *Seminar*, **University of California, Santa Cruz**, California.
73. Seminar, 2009, Seoul National University, Korea.
74. “Memristive Nanodevices”, 2010, *Seminar*, **Peking University**, Beijing, China.
75. “Oxide based nanoswitches”, 2010, *Seminar*, **Chinese Academy of Science**, Beijing, China.
76. “Memristors in Computing: Promises and Challenges”, 2011, *seminar*, **IEEE Computer Society**, San Jose California.
77. “Metal oxide based nonvolatile memories - promises and challenges”, 2011, **IEEE Electronic Device Society**, Santa Clara, California.
78. “Memristive Nanodevices: mechanism, promises and challenges”, 2012, *Seminar*, **University of Pittsburgh**, Pittsburgh, Pennsylvania.
79. “Oxide based Memristive Nanodevices”, 2012, *Seminar*, **Michigan State University**, East Lansing, Michigan.
80. “Mermistor technology development”, 2012, *seminar*, Finisar corp. Sunnyvale California.

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81. “Memristive Nanodevices: Mechanisms, Applications and Challenges”, 2012, **IEEE SINGAPORE REL/CPMT/ED CHAPTER**, Singapore.
 82. “Memristive Devices for Computing”, 2013, **IEEE SCV Electron Devices Society**, Santa Clara, California.
 83. “Memristive nanodevices: mechanisms, promises and challenges”, 2013, *seminar*, **University of California, Berkeley**, California.
 84. *Special Lecture*, **AirForce Research Lab**, Rome, New York (2013). (**Chief Scientist Lecture Series**)
 85. “Memristive materials and Devices”, 2014, *Seminar*, Tsinghua University, Beijing, China.
 86. “Resistance switching: applications, mechanisms and challenges”, 2015, *Seminar*, **HGST**, San Jose, California.
 87. “Challenges and solutions for memristors used for memory and neuromorphic computing”, 2016, *seminar*, **Chinese Academy of Science**, Beijing.
 88. “Memristor applications enabled by selectors”, 2016, *seminar*, **Tsinghua University**, Beijing.
 89. “Diffusive memristor as synaptic emulators for neuromorphic computing”, 2016, *seminar*, **Peking University**, Beijing.
 90. “Memristors for computing”, 2017, *seminar*, Huazhong University of Science and Technology, Wuhan, China.
 91. “Memristive devices for computing: applications, challenges and possible solutions”, 2017, *seminar*, **SUSTC**, Shenzhen, China.
 92. “Memristive devices for computing”, 2017, Micro-Nano Seminar Series, **MIT**, Boston.
 93. “Unconventional computing with memristive devices and arrays”, 2018, Northwestern MRSEC Seminar, **Northwestern University**, USA.
 94. “Unconventional computing with memristive devices and arrays”, 2018, **NIST**, Gaithersburg, Maryland.
 95. “Neuromorphic computing with memristor crossbar arrays”, 2018, Applied Physics colloquium, **Harvard University**, Boston.