Sandip Kundu

Department of Electrical & Computer Engineering
309J Knowles Engineering Bldg
University of Massachusetts
151 Holdsworth Way, Amherst, MA 01003-9284
☎ *+1 (413) 577-3309*
FAX *+1 (413) 545-4628*
✉ *kundu@umass.edu*
http://www-unix.ecs.umass.edu/~kundu

Info

Office Manager: Christine Langlois
langlois@ecs.umass.edu
+1 (413) 545-3621

Education

1984-1988 **PhD** in Electrical and Computer Engineering
Thesis Title: On the Design of Testable CMOS Circuits and Codes for TSC systems
Advisor: Prof. Sudhakar M. Reddy
Department of Electrical and Computer Engineering
University of Iowa
Iowa City, Iowa 52242

1979-1984 **B.Tech**(Hons.) in Electronics and Electrical Communication Engineering
Thesis Title: Design and implementation of a CDMA transceiver
Advisor: Prof. S. L. Maskara
Indian Institute of Technology
Kharagpur, West Bengal 721302, India

Employment

3/2017-present **Program Director** at the National Science Foundation, in the Division of Computer Network Systems, under the Directorate of Computer & Information Science & Engineering

1/2005-present **Professor** in the Department of Electrical & Computer Engineering
University of Massachusetts, Amherst, MA 01003

04/2000-01/2005 **Principal Engineer** at Intel Corporation
AN1-2B17, 1501 S. Mopac, Suite 400, Austin, TX 78746
Includes a semester on sabbatical at University of Freiburg, Germany

07/1997-04/2000 **Senior Component Staff Engineer** at Intel Corporation
2200 Mission College Boulevard, Santa Clara, CA 95052

09/1995-06/1997 **Research Staff Member** at IBM Austin Research Laboratory
MS 9460, 11400 Burnet Road, Austin, TX 78758

05/1988-08/1995 **Research Staff Member** at IBM T. J. Watson Research Center
24-258, PO Box 218, Yorktown Heights, NY 10598
includes a six month temporary assignment at PowerPC design center

Honors and Awards

2015 **Pesquisador Visitante Especial**
Highest level award from Brazil Ministry of Education, for research visit to Federal University of Rio de Janeiro, and other universities, for 6 months, over multiple trips.

2014 **Senior International Scientist** of the Chinese Academy of Sciences
Fellowship at the Institute of Computing Technologies of the Chinese Academy of Sciences

2012 **Senior Faculty Award**
University of Massachusetts at Amherst, College of Engineering

2011 **Best of ATS- 20th Anniversary Compendium**
Efficient BDD-based Fault Simulation in Presence of Unknown Values

2011 Invited Professorship **ENSEIGNANT INVITES**
University of Montpellier, France

2010 **Fellow** of the Japan Society for Promotion of Science

2009 **Best Paper Awards**

1. On Linewidth-based Yield Analysis for Nanometer Lithography, DATE Conference
2. Predictive Thermal Management for Chip Multiprocessors using Co-Designed Virtual Machines, International Conference on High Performance Embedded Architectures Compilers (HiPEAC)

2007 **Fellow of the IEEE**

2006-2009 **Distinguished Visitor** of the IEEE Computer Society

2002 **Most Influential paper in 20 years**
The Best of ICCAD – 20 Years of Excellence in Computer Aided Design, Included in the 20^{th} anniversary compendium of most influential papers in previous 20 year, titled On the design of robust multiple fault testable CMOS combinational logic circuits.

2000 **Intel Development Leadership Pioneer Award**
Highest award in 2000 from the Intel Microprocessor Design Group for a logic and fault simulation system that replaced a hardware accelerated simulator, permitting full chip Pentium IV class design (42M transistors) to be simulated on a single CPU IA-32 machine against defect based fault models. The simulator was demonstrated as a showcase technology by Paul Otellini, Chief Operating Officer of Intel at Design Automation Conference'1999, and by Bill Gates, Chairman of Microsoft Corporation at Intel Microsoft Workstation Leadership forum in Burlingame, CA in 1999.

1996 **IBM Invention Achievement Plateau**
Based on patent count

1994 **IBM Outstanding Technical Achievement Award**
for development of a new Automatic Test Pattern Generation tool which was the first tool capable of handling a million gate design on a state of the art workstation in 1992 with 128M memory at a unsurpassed performance and quality.

1993 **IBM Research Division Award**
for contribution to Logic Synthesis system. The contribution was on removal of redundancy from logic as well as removal of false timing paths. This technology was later licensed to Synopsys Corporation.

1999 **Best Paper in International Conference on Computer Design**

1979 **Government of India National Scholarship**
based on performance at National Talent Search Examination at the end of Secondary School Education.

Major Contributions to Industry

2000 Ultra-drowsy power savings mode in Intel XScale mobile processors: Devised a scheme to save power during state of inactivity which makes it suitable for hand held and wireless applications.
US Patent 6,715,091: System for rearranging plurality of memory storage elements in a computer process to different configuration upon entry into a low power mode of operation

1999 Invented a modeling technology that allows asynchronous circuits to be simulated by synchronous circuit simulators. This allowed Intel Pentium ^{TM}chip to be simulated in its entirety including synchronous, asynchronous, clock-gating and clock distribution systems. The simulator was showcased by Paul Otellini, who was COO of Intel at that time, live, during his keynote speech at Design Automation Conference in 1999. Later, this simulator was also demonstrated by Microsoft Chairman Bill Gates, at Intel Microsoft Workstation Leadership Forum in Burlingame, California on June 30, 1999 as a breakthrough capability. This work resulted in employee award at the highest level (Intel Development Leadership Pioneer Award).
US Patent 6,973,422: Method and apparatus for modeling circuits with asynchronous behavior

1994 Automated extraction of gate level model from transistor level schematic, which could reason through both static signal based circuits as well as pulsed signal (return to zero/ return to one) based circuits. This capability allowed conversion of custom CMOS circuits to gate level model; even in presence of internal feedback, for test pattern generation and circuit verification. This software, called GateMaker^{TM}was acquired by Cadence Corporation from IBM and is used by custom circuit designers.
US Patent 5,629,858: CMOS transistor network to gate level model extractor for simulation, verification and test generation

Major Contributions to Theory

1994 Developed first linear time algorithm for *incremental enumeration* of longest paths; initially used by IBM and NextWave Design Automation Systems in their timing verification product, used in wide array of applications today.

1991 In mid 80s, it was established that many irredundant CMOS circuits are not robustly testable. I proved that for any Boolean function, there exists at least one design implementation that is robustly testable for all CMOS stuck open faults and path delay faults. This is a fundamental result in the design of testable circuits because it establishes that untestability is not tied to function - rather to implementation. This result was first published in International Conference in Computer Design in 1988. In 2002, International Conference in Computer Aided Design (ICCAD) celebrated 20^{th} anniversary with a compendium of most noteworthy papers published in the previous 20 years. This paper was chosen to be included in this compendium for its significance and impact.

1988 Developed the theory of t-Symmetric Error Correcting/All Unidirectional Error Detecting Codes, proving that the resultant codes are decodable and asymptotically optimal, i.e., they become optimal as the code length increases. t-SyEC/AUED codes have found various applications; its use has been acknowledged by the NTT corporation

Research Funding

National Science Foundation, Co-PI, $1,163,227.00, TWC: Medium: Designing Strongly Obfuscated Hardware with Quantifiable Security against Reverse Engineering, with Christof Paar and Daniel Holcomb, 8/1/2016-7/31/2020

Intel Corporation, $300,000.00, 4/2015- open-ended, Embedded Hardware Security Primitives: Low-Cost, Reliable, Unique, Modeling Attack Resistant PUFs and Secure TRNG, Sole-PI

National Science Foundation, Co-PI, $499,997.00, Investigating Stealthy Hardware Trojans, with Christof Paar, 9/1/2014-8/31/2017

National Science Foundation, Co-PI, $265,176.00, Collaborative Research: Eliminating the Energy Efficiency Barrier of Reconfigurable Architectures for Diverse Signal Processing in Mobile Devices, 6/1/2012-5/31/2015

National Science Foundation, PI, $330,000.00, A Design Framework for Improving Reliability, Debug and Security of Multi-Core Systems, 8/1/2009-7/30/2012

Semiconductor Research Consortium, PI, $120,00.00, A Design Framework for Improving Reliability, Debug and Security of Multi-Core Systems, 8/1/2009-7/30/2012

National Science Foundation, PI, $149,621.00, Improving Reliability and Availability of Chip Multiprocessors, 8/1/2008-7/31/2010

Semiconductor Research Consortium, $350,000, 06/01/2006 - 06/31/2010, Thermal Management in Mobile Microprocessors, with Wayne Burleson

National Science Foundation, $100,037, Dynamic hardware adaptation of high performance CMPs for managing thermal hotspots, 10/1/2006-9/30/2008

Semiconductor Research Consortium, $300,000, 07/01/2006 - 06/30/2009, Comprehensive Analysis of Leakage Current in UDSM CMOS Circuits, Sole-PI

Intel Corporation, $80,000 6/2010- open-ended, Design of Error-Tolerant Computing Systems, Sole PI

Intel Corporation, $105,000, 7/2006- open-ended, Error-Tolerant Circuit and System Design, Sole PI, Sponsored by Circuits Research Laboratory, Portland, OR (including supplement in 2007)

Intel Corporation, $165,000, On-Die Circuitry to Enhance Survivability and Observability of Circuit Marginalities, 10/19/2006-open-ended ((including supplement in 2007)

Intel Corporation, $2,694, Computer Equipments, 8/2006

Intel Corporation, $318,000, 1/2006- open-ended, Robust and Low Power Adaptive Clocking Systems for Advanced Microprocessors, with Wayne Burleson (including supplement in 2007)

Intel Corporation, $70,000, 8/2005- open-ended, Application of Diagnosis Techniques to Improve Design for Manufacturing/ DRC, Sole PI, Sponsored by Design Technology Group, Santa Clara, CA (including supplement in 2006)

Intel Corporation, $7,500, Computer Systems Grant, 4/2005

KLA-Tencor Corporation, $260,000, 2/2006- 2/2007, Prolith^{TM}license grant

Teaching

Courses Taught

ECE 232	Hardware Organization and Design
ECE 242	Introduction to Data Structures
ECE 353	Computer Systems Lab I
ECE 354	Computer Systems Lab II
ECE 373	Software Intensive Engineering
ECE 654	Testing and Diagnosis of VLSI Systems
ECE 697pp	Design for Manufacturability and Reliability of VLSI Circuits
ECE 558	Introduction to VLSI Design
ECE 559	VLSI Design Project
ECE 658	VLSI Design Principles
ECE 659	Advanced VLSI Design Project

Significant Curriculum Development

ECE 654	Developed from scratch.
ECE 697pp	Developed from scratch.
ECE 354	Significantly altered labs with new components.
ECE 353	Introduced UNIX components. New submission system.

Nominated for Distinguished Teaching Awards

In years 2010, 2009, 2006

Students

Post-Doctoral

2007-2009 Hyunbean Yi, PhD, Computer Science & Engineering, Hanyang University
Currently an Assistant Professor at Hanban National Univeristy, Daejeon, Korea

Doctoral

current Vinay Patil on Hardware Security
current Mohammed Nazmul Islam on Hardware Security
2016 Arunkumar Vijayakumar on Hardware Security
2016 Sudarshan Srinivasan on Low Power Architecture
2013 Rance Rodrigues, nVIDIA Corporation
2011 Kunal Ganeshpure, Mentor Graphics Corporation
2010 Aswin Sreedhar, Intel Corporation
2010 Alodeep Sanyal, Synopsys
2009 Omer Khan, Assistant Professor, University of Connecticut, Storrs

Masters

2015 Nithesh Kurella, Samsung
2013 Bharath Phanibhushana, Netronome
Arunachalam Annamalai, AMD
2012 Nishant Dhumane, Broadcom Corporation
2011 Lokesh Subramany, Global Foundries
Michael Buttrick, Intel Corporation
2010 Shruti Vyas, Intel Corporation
Spandana Remarsu, Intel Corporation
2009 Nagraj Kelageri, Qualcomm Corporation
Abhisek Pan, continued to PhD
Rance Rodrigues, continuing to PhD
2008 Aarti Choudhary, Intel Corporation
2007 Kunal Ganeshpure, continued to PhD
Tariq Bashir Ahmed, continued to PhD
Aswin Sreedhar, continued to PhD
Ashesh Rastogi, Intel Corporation
Atchuthan S Perinkulam, Vonage Corporation
2006 Tom Nielson, BAE Systems
Joe Brackett, BAE Systems

Professional Activities

Journal Editor

2015 Guest Editor, Joint Special Section on Defect and Fault Tolerance in VLSI and Nanotechnology Systems and *IEEE Transactions on Computers* and *IEEE Transactions on Nanotechnology*

2015 Guest Editor, *IEEE Transactions on Emerging Topics in Computing* Special Section on ISVLSI

2013 Guest Editor, Design methodologies for Nanoelectronic Digital and Analogue Circuits, *IET Transactions on Circuits, Devices and Systems*

2014-date Associate Editor, *IEEE Transactions on Dependable and Secure Computing*

2012-2014 Associate Editor, *ACM Transactions on Design Automation of Electronic Systems*

2007-2009 Associate Editor, *IEEE Transactions on VLSI*

2007 Guest Editor, *IEEE Transactions on VLSI Systems* Special Section on Autonomous silicon Validation and Testing of Microprocessors and Microprocessor-based Systems

2002-2007 Associate Editor, *IEEE Transactions on Computers*

Conference Steering Committee

2013-date IEEE Computer Society Annual Symposium on VLSI (ISVLSI)

2013-date IEEE Internal Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFTS)

2011-date International Conference on Computer Design (ICCD)

Conference General Chair/Co-Chair

2005 28th IEEE Defect and Fault Tolerance in VLSI and Nanotechnology Systems Symposium, (DFTS 2015)

2005 18th International Conference in VLSI Design, (VLSI 2005)

2005 TTTC Technical Forum on Meeting Time To Volume Challenges

2001 International Conference in Computer Design (ICCD 2001)

Conference Technical Program Chair/Co-Chair

2014 International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFTS 2014)

2014 IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2014)

2012 IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2012)

2001 Asian Test Symposium (ATS 2011)

2000 International Conference in Computer Design (ICCD 2000)

Conference Keynote Speaker

2016 IEEE International Symposium on Nanoelectronic and Information Systems, Indore, India

2008 Design and Diagnostics of Electronic Components and Systems, Bratislava, Slovak Republic

2008 DATE Workshop on the Impact of Process Variability on Design and Test, Munich

2005 Testmethoden und Zuverlassigkeit von Schaltungen und Systemen, Innsbruck, Austria, 2005

2000 DCIS'2000, Montpellier, France

2000 Testmethoden und Zuverlassigkeit von Schaltungen und Systemen, Grassau, Germany

Conference Panelist

2014 Design Automation Conference
2009 Design Automation Conference
2004 International Test Synthesis Workshop
2004 Design Automation and Test Conference
2000 International Test Conference
1998 International Test Conference
1996 International Conference in Computer Design
1995 Asian Test Symposium
1993 IEEE VLSI Test Symposium

Conference Technical Program Committee Member

International Conference in Computer-Aided Design
Design Automation Conference
Design Automation and Test in Europe
International Conference in Computer Design
Asian Test Symposium
European Test Symposium
ISVLSI, SPIE, DELTA, IOLTS, DFTS and many others

Semiconductor Research Consortium

2001 Author of a White Paper
1998-2005 Intel Representative
1998 AB member: Design Verification
1995-1997 IBM Representative
1996 Task force member of Test sub-committee for goal setting

National Science Foundation

2000-2016 Panelist

Recent Invited Talks

1. Keynote, "Securing Vehicle Passengers from Cyber Threats: Covert and Overt," Internet of Things (IoT) and Automotive Security Workshop (IASW) held in conjunction with IEEE International Symposium on Hardware Oriented Security and Trust (HOST), McLean, VA, May 5, 2017
2. Keynote, "Securing Physically Unclonable Functions," 26th North Atlantic Test Workshop, Providence, RI, May 10, 2017
3. Keynote, "On Securing the Internet-of-Things:One PUF at a time," 3rd Brazil Workshop on Microarchitectural Challenges: Performance, Energy Efficiency and Resilience, Rio de Janeiro, Brazil, `http://wmc2017.ime.uerj.br/program.html`, March 17, 2017
4. Graduate colloquium, "Exploring Heterogeneity within a Core for Improved Power Efficiency," TU Dresden, Germany, December 22, 2016
5. Graduate colloquium, "Securing Physically Unclonable Functions," Ruhr University Bochum, Germany, December 15, 2016
6. Distinguished Lecture at the State University of Rio de Janeiro, Brazil, "Improving Yield and Reliability of Chip Multiprocessors," March 30, 2015
7. Distinguished Lecture at the Federal University of Rio Grande do Sul, "Improving Yield and Reliability of Chip Multiprocessors," March 19, 2015
8. Improving Yield and Reliability of Chip Multiprocessors, Invited Speaker at Tsinghua University, Beijing, China, May 8, 2014
9. Adaptive Thread to Core Assignment via Online Program Phase Classification in Asymmetric Multicore Processors (AMP), Distinguished Lecture at Chinese Academy of Sciences, Beijing, China, March 10, 2014
10. Adaptive Thread to Core Assignment via Online Program Phase Classification in Asymmetric Multicore Processors (AMP), Invited Speaker at Chalmers Institute of Technology, Sweden, May 27, 2013
11. Adaptive Thread to Core Assignment via Online Program Phase Classification in Asymmetric Multicore Processors (AMP), Invited Speaker at Bristol University, UK, May 24, 2013
12. Adaptive Thread to Core Assignment via Online Program Phase Classification in Asymmetric Multicore Processors (AMP), Invited Speaker at Southampton University, UK, May 22, 2013
13. Error Resilient Processor Design, Invited Speaker at University of Passau, Germany, July 25, 2011
14. "Improving Performance and Yield via Physical Design Changes Reasoned Solely from Tester Response," Global Foundries, Milpitas, CA, June 10, 2011
15. Error Resilient Processor Design, Invited Speaker at École Polytechnique Fédérale De Lausanne, Switzerland, June 6, 2011
16. Sub-wavelength Lithography: Current Practices, Impact of Process Variation, Defect Modeling, Invited Speaker at Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier, France, May 30, 2011
17. Graduate Colloquium at Georgia Tech, Atlanta, GA, April 8, 2011
18. Invited speaker at Intel Corporation, Hillsboro, OR, April 1, 2011
19. Invited speaker at University of Tokyo, Tokyo, Japan, June 2010

20. Invited talk at Semiconductor Technology Advance Research Corporation, Yokohama, Japan, June 2010
21. Invited speaker at Nara Advanced Institute of Science and Technology, Nara, Japan, June 2010
22. Invited speaker at Kyushu Institute of Technology, Kyushu, Japan, June 2010
23. Invited talk on Low Power Processor Design, Intel Corporation, May 29, 2009
24. Invited talk on Low Power Processor Design, Qualcomm Corporation, May 21, 2009
25. Keynote Speech at DATE Workshop on the Impact of Process Variability on Design and Test, Munich, 2008 (http://www.date-conference.com)
26. Keynote Speech at Design and Diagnostics of Electronic Components and Systems, Bratislava, Slovak Republic, 2008 (http://ui.sav.sk/DDECS2008/)
27. Invited Talk at International Symposium on VLSI Design and Test, Hsinchu, Taiwan, 2008 (http://vlsidat.itri.org.tw/2008/General/)
28. Virtual Thermal Management: An Alternative to Dynamic Voltage and Frequency Scaling, University of Newcastle, Newcastle, UK, August 4, 2008
29. Placement of Post Silicon Clock Tuning Buffers for Mitigating the Impact of Process Variation, ARM Research Lab, Cambridge, UK, July 29, 2008
30. Design for Manufacturability and Reliability, National Taiwan University, Taipei, Taiwan, August 29, 2007
31. On Testing Circuit Marginalities, National Tsing-Hua University sponsored education course, Hsinchu, Taiwan, August 27, 2007
32. IEEE Distinguished Lecture on Design for Manufacturability, Linkoping, Sweden, October 1, 2007
33. IEEE Distinguished Lecture on Design for Manufacturability, Tallinn, Estonia, October 3, 2007

Publications

Books, Book Chapters

1. Sandip Kundu and Aswin Sreedhar, "Nanoscale CMOS VLSI Circuits: Design for Manufacturability," ISBN: 978-0071635196, McGraw-Hill Professional, 2010

2. Sandip Kundu and Alodeep Sanyal, Introduction Chapter in "Power-Aware Testing and Test Strategies for Low Power Devices," Edited by Patrick Girard, Nicola Nicolici, Xiaoqing Wen, ISBN: 978-1-4419-0927-5, Springer, 2009

3. Omer Khan, Sandip Kundu, "Predictive Thermal Management for Chip Multiprocessors Using Co-designed Virtual Machines,", Book Series Lecture Notes in Computer Science, Springer, ISSN 0302-9743, ISBN 978-3-540-92989-5, 2009

4. Niraj Jha and Sandip Kundu, "Testing and Reliable Design of CMOS Circuits," ISBN 0-7923-9056-3, TK7871.99.M44J49, Kluwer Academic Publishers, Boston, MA, 1990

5. Sudhakar Reddy and Sandip Kundu, "Fault Detection and Design for Testability of CMOS Logic Circuits," Chapter in "Testing and Diagnosis of VLSI and ULSI" Edited by F. Lombardi and M. G. Sami(Eds), pp. 69-92, Kluwer Academic Publishers, Boston, MA, 1988

Journals

1. Tiago Alves, Leandro A. J. Marzulo, Felipe M. G. França and Sandip Kundu, "Concurrency Analysis in Dynamic Dataflow Graphs," IEEE Transactions on Emerging Topics in Computing, (accepted) 2017

2. Md. Nazmul Islam, Vinay C Patil, Sandip Kundu, "A Guide to Graceful Aging: How Not to Overindulge in Post-Silicon Burn-in for Enhancing Reliability of Weak PUF," IEEE Transactions on Circuits and Systems II, (accepted) 2017

3. Vijayakumar, Arunkumar, Vinay C. Patil, and Sandip Kundu. "On Improving Reliability of SRAM-Based Physically Unclonable Functions," Journal of Low Power Electronics and Applications 7,1 (2017): 2. `http://www.mdpi.com/2079-9268/7/1/2/htm`

4. Arunkumar Vijayakumar, Vinay C. Patil, Daniel E. Holcomb, Christof Paar, and Sandip Kundu, "Physical Design Obfuscation of Hardware: A Comprehensive Investigation of Device and Logic-Level Techniques," IEEE Transactions on Information Forensics and Security, vol. 12, no. 1, pp. 64-77, Jan. 2017.

5. Jian Wang, Huawei Li, Tao Lv, Tiancheng Wang, Xiaowei Li and Sandip Kundu, "Abstraction-Guided Simulation Using Markov Analysis for Functional Verification," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 35, no. 2, pp. 285-297, Feb. 2016

6. Sudarshan Srinivasan, Nithesh Kurella, Israel Koren, Sandip Kundu. "Exploring Heterogeneity within a Core for Improved Power Efficiency," IEEE Transactions on Parallel and Distributed Systems, vol. 27, no. 4, pp. 1057-1069, April 1 2016

7. Vikram B. Suresh, Sandip Kundu, "Managing Test Coverage Uncertainty due to Random Noise in nano-CMOS: A Case-Study on an SRAM Array," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), vol. 35, no.1, pp.155-165, Jan. 2016

8. R.Rodrigues, I.Koren and S.Kundu, "Does the Sharing of Execution Units Improve Performance/Power of Multicores?," ACM Transactions on Embedded Computing Systems (TECS), Volume 14, Issue 1, Article No. 17, January 2015

9. Abhisek Pan, Rance Rodrigues and Sandip Kundu, "A Hardware Framework for Yield and Reliability Enhancement in Chip Multiprocessors," ACM Transactions on Embedded Computing Systems (TECS), Volume 14, Issue 1, Article No. 12 , January 2015

10. Kunal Ganeshpure and Sandip Kundu, "Performance-driven dynamic thermal management of MPSoC based on task rescheduling," ACM Trans. Des. Autom. Electron. Syst. 19, 2, Article 11 (March 2014), 33 pages.

11. Aida Todri, Sandip Kundu, Patrick Girard, Alberto Bosio, Luigi Dilillo, Arnaud Virazel, "Globally Constrained Locally Optimized 3D Power Delivery Networks," IEEE Transactions on VLSI Systems, vol.22, no.10, pp.2131-2144, Oct. 2014

12. R. Rodrigues, A. Annamalai, and S. Kundu. "A Low Power Instruction Replay Mechanism for Design of Resilient Microprocessors". ACM Transactions on Embedded Computing Systems (TECS) Article 85, 23 pages, March 2014

13. R.Rodrigues, A.Annamalai, I.Koren and S.Kundu, "A Study on the use of Performance Counters to Estimate Power in Microprocessors," IEEE Transactions on Circuit and Systems II: Express Briefs, vol.60, no.12, pp.882,886, Dec. 2013

14. Kunal Ganeshpure and Sandip Kundu, "Game theoretic Approach for Run-time Task Scheduling on an MPSoC," IET Circuits, Devices and Systems 7.5 (2013): 243-252.

15. A. Todri, S. Kundu, P. Girard, A. Bosio, L. Dilillo, A. Virazel, "A Study of Tapered 3D TSVs for Power and Thermal Integrity," IEEE Transactions on VLSI, Feb. 2013, pp. 306-319

16. Rance Rodrigues, Arunachalam Annamalai, Israel Koren, and Sandip Kundu, "Improving performance per watt of asymmetric multi-core processors via online program phase classification and adaptive core morphing," ACM Transactions on Design Automation of Electronic Systems, Vol. 18, No. 1, pp. 5:1-5:23, January 2013

17. Alodeep Sanyal, Kunal Ganeshpure, Sandip Kundu, "Test Pattern Generation for Multiple Aggressor Crosstalk Effects Considering Gate Leakage Loading from Fanout Nodes in Presence of Gate Delays," IEEE Transactions on VLSI, vol. 20, number 3, 2012, pp. 424-436.

18. Aswin Sreedhar, Sandip Kundu and Israel Koren, "On Reliability Trojan Injection and Detection," Journal of Low Power Electronics, vol 8, number 5, 2012, pp. 674-683

19. Omer Khan and Sandip Kundu, "An Empirical Model for Cooperative Resizing of Processor Structures to Exploit Power-Performance Efficiency at Runtime," Journal of IET Circuits, Devices and Systems, September 2012, pp. 355 - 365

20. Sudarshan Srinivasan, Kunal P Ganeshpure, Sandip Kundu, "A Wavelet based Spatio-Temporal Heat Dissipation Model for Reordering of Program Phases to Produce Temperature Extremes in a Chip," Vol. 31, No. 12, pp. 1867-1880, December 2012.

21. Kunal Ganeshpure, Alodeep Sanyal and Sandip Kundu, "A Pattern Generation Technique for Maximizing Switching Supply Currents Considering Gate Delays," IEEE Transactions on Computers, vol. 61, no. 7, pp. 986-998, July 2012

22. Michael Buttrick, Sandip Kundu, "On Testing Prebond Dies with Incomplete Clock Networks in a 3D IC Using DLLs," Journal of Electronic Testing, vol. 28, pp: 93-101, Feb 2012

23. Omer
in Chip Multiprocessors," IEEE Transactions on Dependable and Secure Computing, pp. 714-727, September/October, 2011.

24. Omer Khan and Sandip Kundu, "Microvisor: A Runtime Architecture for Thermal Management in Chip Multiprocessors," Transactions on High-Performance Embedded Architectures and Compilers, Volume 4, LNCS 6760, pp. 84-110, 2011

25. Alodeep Sanyal, Syed M. Alam and Sandip Kundu, "Built-In Self-Test for Detection and Characterization of Transient and Parametric Failures," IEEE Design and Test, vol 27, number 5, 2010, Pages 50-59

26. Debasis Mitra, Susmita Sur-Kolay, Bhargab B. Bhattacharya, Sandip Kundu, Ashish Nigam, Sandeep K. Dey, "Test Pattern Generation for Droop Faults," IET Comput. Digit. Tech, vol 4, 2010, Pages 274-284

27. Omer Khan, Sandip Kundu, "Thread Relocation: A Runtime Architecture for Tolerating Hard Errors in Chip Multiprocessors," IEEE Transactions on Computers, pp. 651-665, May, 2010.

28. Alodeep Sanyal, Ashesh Rastogi, Wei Chen, Sandip Kundu. "An Efficient Technique for Leakage Current Estimation in Nano-Scaled CMOS Circuits Incorporating Self-loading Effects," IEEE Transactions on Computers, vol 59, number 7, 2010, Pages 922-932

29. Kunal P. Ganeshpure and Sandip Kundu, "On ATPG for Multiple Aggressor Crosstalk Faults,", IEEE Transactions on CAD, vol. 29, pp. 774-787, May 2010

30. Hyunbean Yi, Sungju Park, and Sandip Kundu, "On-Chip Support for NoC-based SoC Debugging," IEEE Transactions on Circuits and Systems I, vol 57, number 7, 2010, Pages 1608-1617

31. Hyunbean Yi, Sandip Kundu, S. Cho and S. Park, "A Scan Cell Design for Scan-based Debugging of an SoC with Multiple Clock Domains, IEEE Transactions on Circuits and Systems II, vol 57, No 7, 2010, Pages 561-565

32. R. A. Shafik, B. M. Al-Hashimi, S. Kundu, A. Ejlali, "Soft Error-Aware Voltage Scaling Technique for Power Minimization in Application-Specific MPSoC," Journal of Low Power Electronics, August 2009

33. Alodeep Sanyal, Kunal Ganeshpure, Sandip Kundu, " An Improved Soft Error Rate Measurement Technique," IEEE Trans. on CAD, pp. 596-600, April 2009

34. Aswin Sreedhar, Sandip Kundu, "Lithography Simulation Basics and a Study on Impact of Lithographic Process Window on Gate and Path Delays," Journal of Low Power Electronics, 4, 392–401 (2008)

35. Ashesh Rastogi, Kunal P. Ganeshpure, Alodeep Sanyal, Sandip Kundu, "On Composite Leakage Current Maximization,", Journal of Electronic Testing: Theory and Applications (JETTA), pp. 405-420, Volume 24, Number 4, August, 2008

36. Piet Engelke, Ilia Polian. Michel Renovell, Sandip Kundu, Bernd Becker, Bharath Seshadri, and Irith Pomeranz, "On Detection of Resistive Bridging Defects by Low-Temperature and Low-Voltage Testing," IEEE Trans. on CAD of Integrated Circuits and Systems 27(2): 327-338 (2008)

37. Ilia Polian, Alejandro Czutro, Sandip Kundu, Bernd Becker, "Power Droop Testing," IEEE Design and Test of Computers, vol. 24, no. 3, pp. 276-284, May-June, 2007

38. Sandip Kundu, Aswin Sreedhar, Alodeep Sanyal, "Forbidden pitches in Sub-Wavelength Lithography and their Implications on Design," The Journal of Computer-Aided Materials Design, ISSN: 0928-1045, Vol. 14, No 1, 2007, pp. 79-89

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3. Leandro Santiago, Vinay C Patil, Sandip Kundu, Felipe M. G. Fraça, Charles B. Prado, Tiago A. O. Alves and Leandro A. J. Marzulo, "Realizing Strong PUF from Weak PUF via Neural Computing," 2017 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), 2017

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