ECE 568/668 – Computer Architecture
College of Engineering
Electrical and Computer Engineering Department
Fall 2019

General

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Catalog Description

Quantitative study of pipelined processor architectures, memory hierarchy, cache memory, Input/Output, RISC processors and vector machines.

Course Overview

The goal of this course is for students to better understand the interaction between software and hardware and know how hardware is designed so as to provide the required functionality at the highest possible performance. The course begins with basic processor design and proceeds to advanced concepts implemented in modern microprocessors. We cover pipelining, superscalar, speculative and out-of-order execution, vector units, VLIW machines and multithreading. We also cover the design principles of memory systems including virtual memory, cache units, DRAM and storage systems like hard drives and Solid-state drives. We conclude with high-level performance analysis of input/output systems. The course emphasizes quantitative evaluation of the benefits and cost of all the performance enhancement techniques that are currently integrated into modern processor.

Course Learning Objectives

- Develop an understanding of computer architecture and performance measures
- Analyze characteristics of pipelines, control signals, datapaths, and control hazards
- Demonstrate understanding of various types of scheduling
- Explore various types of prediction and branch handling schemes
- Analyze techniques, advantages, and disadvantages related to types of compilers
- Compare types of memory and input/output systems

Course Requirements &Prerequisites

ECE 112 and ECE 232 (331) or equivalent courses in Digital Design and Hardware Organization

Course Materials

Required Text:

Hennessy, J. L., & Patterson, D. A. (2019). *Computer architecture: A quantitative approach* (6th ed.), Elsevier, ISBN: 978-0-12-811905-1 (5th. ed. “2012” is OK)

Recommended Resources:

1) Flynn, M. J. (1995). *Computer architecture: Pipelined and parallel processor design*. Boston, MA: Jones and Bartlett. Heuring, V. P, & Jordan, H. F. (2004). *Computer systems design and architecture* (2nd ed.). Upper Saddle River, NJ: Pearson.
2) Hwang, K. (1993). *Advanced computer architecture: Parallelism, scalability, programmability*. New Delhi: McGraw- Hill.
3) Shen, J. P., & Lipasti, M. H. (2005). *Modern processor design: Fundamentals of superscalar processors*. Long Grove, IL: McGraw-Hill.

Recommended Technical Papers

- Davidson, E. S., Shar, L. E., Thomas, A. T., & Patel, J. H. (n.d.). Effective control for pipelined computers. 181–184.
- Hinton, G., Sager, D., Upton, M., Boggs, D., Carmean, D., Kyker, A., & Roussel, P. (2001). The microarchitecture of the Pentium® 4 processor. *Intel Technology Journal*, *Q1*, 1–13.
- McFarling, S. (1993). WRL technical note TN-36: Combining branch predictors. *Digital Equipment Corporation*.
- Smith, J. E., & Pleszkun, A. R. (1988). Implementing precise interrupts in pipelined processors. *IEEE Transactions on Computers*, *37*(5), 562–573.
- Srinivasan, S. K., & Velev, M. N. (2003). Formal verification of an Intel XScale processor model with scoreboarding, specialized execution pipelines, and imprecise data-memory exceptions. *Formal Methods and Models for Codesign (MEMOCODE '03)*, 65–74.

Course Grading

Midterm 1:	After Lecture 12	(Fri. Oct. 11, 5:00- 7:00pm - Tentative)	80 Points
Midterm 2:	After Lecture 20?	(Fri. Nov. 15, 5:00- 7:00pm - Tentative)	80 Points
Final:	After Lecture 26	(Wed. Dec. 18, 3:30- 5:30pm)	100 Points
Quizzes and Class participation:		(568 Students)	100 Points
Quizzes and ????? :		(668 Students)	100 Points
Total:			360 Points

Your Grade	Your Total Points
A	335-360
A-	320-334
B+	305-319
B	290-304
B-	275-289
C+	260-274
C	245-259
C-	230-244
D+	215-229
D	195-210
D-	180-194
F	179 or less

Outline:

I. Introduction
II. Performance Analysis (Ch.1+)
III. Processor Design: Instruction-level Parallelism, Pipelining (App. C, Ch.3)
IV. Memory Design: Memory Hierarchy, Cache Memory, Secondary Memory (App. B, Ch.2)
V. Storage systems and Input/Output (App. D)
VI. Vector Computers and GPUs (Ch.4) [Time permitting]

Credits

This course is worth 3 credits.

Attendance

Students are expected to attend all regularly scheduled classes. In cases of illness, students are to explain their absences directly to the instructor. The grades of students who have met the requirements of the instructor in making up their work shall not be reduced for absence because of illness. Students are not to be penalized for official off-campus trips.

Academic Honesty

Students should demonstrate **their own** learning during examinations and other academic exercises, and that other sources of information or knowledge be appropriately credited. No form of cheating, plagiarism, fabrication, or facilitating of dishonesty will be condoned in this class.

Useful Links

WWW Computer Architecture Page

Inclusivity

The diversity of the participants in this course is a valuable source of ideas, problem solving strategies, and engineering creativity. If you feel that your contribution is not being valued or respected for any reason, please speak with me privately. If you wish to communicate anonymously, you may do so in writing, speak with Assistant Dean Paula Rees (rees@umass.edu, 413.545.6324, Marston 128), or submit your concern through the College or Engineering Climate Concerns and Suggestions on-line form (tinyurl.com/UMassEngineerClimate). We are all members of an academic community with a shared responsibility to cultivate a climate where all students/individuals are valued and where both they and their ideas are treated with respect.

Disclaimer

The materials on this syllabus by no means, direct or indirect, should be interpreted as complete and comprehensive. When in doubt contact the instructor for clarifications. Also, the instructor reserves the rights to make changes to the items on this syllabus as found appropriate for better learning of the course materials by the students. Such changes will be immediately communicated to the students in class and via Email.