CURRICULUM VITAE
Yadi Eslami

Email : yeslami@ieee.org

➢ EDUCATION:

2005 Ph.D., Department of Electrical and Computer Engineering, University of Toronto, Canada. Dissertation Title: *Ferroelectric Memory Design and its application to Universal Cryptography Processors*

1987 M.Sc., Communication Systems, Department of Electrical and Computer Engineering, Isfahan University of Technology, Isfahan, Iran

1985 B.Sc., Electrical and Electronics Engineering, Engineering School, Shiraz University, Shiraz, Iran

➢ TEACHING AND RESEARCH INTERESTS:

- Reconfigurable processor architectures
- Special purpose processors
- Digital circuits and systems
- VLSI memories

➢ ACADEMIC EXPERIENCE:

September 2017 – Present: Senior Lecturer

University of Massachusetts, Amherst, Electrical and Computer Engineering Department, Amherst, Massachusetts
Responsibilities include teaching graduate level Computer Engineering courses: Computer Networks and Computer Architecture

January 2016 – Augustb2017: Assistant Professor

West Virginia University Institute of Technology, Department of Electrical and Computer Engineering, Montgomery, West Virginia
Responsibilities include teaching Digital Logic Design, Microprocessors Systems, Computer Architecture, VLSI Design, and VHDL Design courses and running their Laboratories

August 2010 – December 2015: Assistant Professor

West Virginia University Institute of Technology, Department of Engineering Technology, Montgomery, West Virginia
Responsibilities include teaching Digital Systems and Microprocessors, Programmable Logic Controllers, Control System Technology, Electronic Measurements and Instrumentations, Communication Systems, and Microprocessor-based data acquisition systems and control courses and conducting the Laboratory component of these courses

January 2010 – August 2010: Adjunct Faculty

College of Western Idaho, Department of Business and Economics, Nampa, Idaho, USA.
Responsibilities include teaching Pre-algebra and College Algebra

1999 – 2005: Teaching Assistant

Department of Electrical and Computer Engineering, University of Toronto, Toronto, Canada.
Responsibilities included implementing tutorials, conducting labs, marking exams and homework. Courses addressed included Digital Systems, Digital Electronics, Computer Organization, and Computer Hardware.

1986 – 1999: Lecturer

Department of Electrical and Computer Engineering, Isfahan University of Technology, Isfahan, Iran.
Courses taught included Signal and Systems, Analog Communications Systems, Digital Communication Systems, Digital Design, Digital Computer Architecture, Advanced Digital Design, Microprocessors-I (8 and 16-Bit), Microprocessors-II (32-Bit Microprocessors & Microcontrollers), Computer Interfacing. Developed Digital Design and Microprocessors laboratory modules.
Supervised B.Sc. projects, including Wireless Mouse, MCS8751-52 Microcontroller Trainer, Matrix LED display controller, EPROM Programmer, EEPROM Programmer.

➢ INDUSTRIAL EXPERIENCE:

February 2005 – June 2009

Design Engineer, DRAM R&D, Micron Technologies Inc., Boise, Idaho, USA. Responsibilities included design, simulation, and optimization of major DDR3 SDRAM building blocks. Major accomplishments included the following: (1) Proposed and implemented circuit techniques that reduced the DDR3 DRAM chips power consumption by 10%, employed in the DDR3 line of products at Micron. (2) Proposed a software package for DRAM designers to inspect the power consumption of various DRAM blocks from each power rail, and after approval, directed a CAD group to implement it. It is a part of the standard design flow at Micron now. (3) Analyzed and proposed modifications for DDR3 DRAM chips Power Buses and proposed the power bus characteristics that reduce the output data jitter. (4) Modified the existing DDR3 Input Buffer circuit for faster and more symmetric operation – A US patent is filed for this innovation. (5) Designed a fast Input Buffer circuit to operate at (estimated) DDR4 speed (1.6GHz, 200ps Pulse width), to be used in the DDR4 line of products at Micron. (6) Studied and simulated new Data Path implementation techniques for further power reduction of DDR3 DRAM.

June 2005 – August 2006

System Design Engineer (part-time), SciTech AAG, Inc., Toronto, Ontario, Canada. Responsibilities included design, simulation, and prototyping of a data acquisition and

processing system based on TI TMS320C6713 DSP. Major accomplishments included the following: (1) Piezoelectric transducer modeling. (2) Schematic design and simulation of digital and analog blocks. (3) Verification and optimization of all blocks. (4) Programming the DSP using the Code Composer Studio package provided by TI. (5) Integration, bring-up, test, and documentation of the final product.

➢ PROFESSIONAL MEMBERSHIPS:

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- Sept.2017 – Present IEEE member, ASEE member
- 2014 – Aug. 2017 IEEE West Virginia Section Vice-Chair, ASEE member
- 2013 IEEE West Virginia Section Chair
- 2011-2012 IEEE West Virginia Section Vice-Chair
- 2005 – Present IEEE member
- 1999 – 2005 IEEE student member
- 1983 – 1987 IEEE student member

➢ SCHOLARSHIPS:

- 2002-2003 Ontario Graduate Scholarship (OGS)
- 2001-2002 Edward S. Rogers Sr. Departmental Scholarship
- 1999-2002 University of Toronto Fellowship

➢ IMMIGRATION STATUS:

- Legal Permanent Resident (Green Card Holder)

➢ PUBLICATIONS:

Refereed Journals

K. Sedghisigarchi , **Y. Eslami,** A. Davari, "A Low-cost Efficient Hardware-in-the-loop Testbed for Distributed Generation Penetration Analysis," Accepted by the *Journal of Energy and Power Engineering*, Dec. 2016

K. Sedghisigarchi , **Y. Eslami,** A. Davari, "A Real-time Power Controller for Grid-connected inverters in LV Smart Microgrids," *Journal of Energy and Power Engineering.* vol. 7, no. 11, pp. 2156-2163, Nov. 2013

Y. Eslami, A. Sheikholeslami, P. G. Gulak, S. Masui, T. Endo, and S. Kawashima, "A universal reconfigurable cryptography processor for smart cards," *IEEE Transactions on VLSI Systems*, vol. 14, no. 1, pp.43 – 56, Jan. , 2006.

Y. Eslami, A. Sheikholeslami, S. Masui, T. Endo, and S. Kawashima, "Circuit implementations of the Differential Capacitance Read- Scheme (DCRS) for Ferroelectric Random-Access Memories (FeRAMs)," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 11, pp. 2024 - 2031, Nov. 2004.

J. W. K. Siu, **Y. Eslami,** A. Sheikholeslami, P. G. Gulak, T. Endo, and S. Kawashima, "A current-based reference-generation scheme for 1T-1C Ferroelectric Random-Access Memories," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 3, pp. 541-549, Mar. 2003.

Refereed Conferences

Felipe A. A. R. Sozinho, Kenan Hatipoglu , **Yadollah Eslami-Amirabadi**, Asadollah Davari, "HARDWARE IMPLEMENTATION OF A MICROGRID CONTROLLER FOR ENHANCING DYNAMIC VOLTAGE STABILITY," Submitted to IEEE PES General Meeting, Nov. 2016.

K. Sedghisigarchi , **Y. Eslami,** A. Davari, "A Real Time HIL Testbed for Distributed Energy Generation Penetration Analysis", in IEEE International Energy Conference, ENERGYCON 2016, Apr 04-08, 2016, Leuven, Belgium.

K. Sedghisigarchi , **Y. Eslami,** A. Davari, "A Real-Time Testbed for Coordinated Control of Inverters in LV Microgrids " in IEEE International Energy Conference, ENERGYCON 2014, May 13-16, 2014, Dubrovnik, Coratia,

K. Sedghisigarchi , **Y. Eslami,** A. Davari, "A Real-time Power flow Controller for Grid-connected Converters in LV Microgrids, " in 2012 CIGRE Canada Conference: Technology and Innovation for the Evolving Power Grid, Sept. 24-26, 2012, Montreal, Quebec, Canada

Y. Eslami, M. Al-Nasra, T. Abu-Lebdeh "Power-aware and self-sustainable data acquisition/monitoring/logging stations for acidic drainage monitoring of abandoned coal mines," in *The 2nd International Conference on Green & Sustainable Technology,* 2011, Greensboro, NC, USA.

Y. Eslami, A. Sheikholeslami, S. Masui, T. Endo, and S. Kawashima, "A Differential-Capacitance Read Scheme for FeRAMs," in *Symposium on VLSI Circuits, Digest of Technical Papers*, 2002, Honolulu, HI, USA, pp. 298-301.

J. W. K. Siu, **Y. Eslami,** A. Sheikholeslami, P. G. Gulak, T. Endo, and S. Kawashima, "A 16kb 1T1C FeRAM testchip using current-based reference scheme," in *IEEE Custom Integrated Circuits Conference*, CICC-2002, May 12-15, 2002, Orlando, Florida, USA, pp. 107-110.

Y. Eslami, J. W. K. Siu, A. Sheikholeslami, P. G. Gulak, T. Endo, and S. Kawashima, "A 2T-2C FeRAM testchip for optimum bitline and cell capacitances," in *1st International meeting on Ferroelectric Random Access Memories*, Extended Abstracts, Nov. 2001, Gotemba, Japan, pp. 178-179.

➢ PATENTS:

S. Masui, **Y. Eslami**, and A. Sheikholeslami,
Ferroelectric memory supplying predetermined amount of direct-current bias electricity to first and second bitlines upon reading data from memory cell,
Canadian Patent No. 2,430,875, issued on Feb. 5, 2008.
This patent is acquired by Fujitsu Laboratories Limited, Kawasaki, Japan.

S. Masui, **Y. Eslami**, and A. Sheikholeslami,
Plate line non-drive improved reading method for a ferroelectric memory,
European Patent No. 1,369,876, granted on March 14, 2007.
This patent is acquired by Fujitsu Laboratories Limited, Kawasaki, Japan.

Y. Eslami
Symmetrically operating single-ended input buffer devices and methods,
US Patent Application No. 13/796,998, Disclosure No.: 2006-1010.03/US
This patent is acquired by Micron Technology, Inc., Boise, ID, USA.

S. Masui, **Y. Eslami**, and A. Sheikholeslami,
Ferroelectric memory supplying predetermined amount of direct-current bias electricity to first and second bitlines upon reading data from memory cell,
US Patent No. 6,882,559, issued on Apr. 19, 2005.
This patent is acquired by Fujitsu Laboratories Limited, Kawasaki, Japan.